COMPACT INTEGRATED TRANSCONDUCTANCE AMPLIFIER CIRCUIT FOR TEMPORAL DIFFERENTIATION

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ABSTRACT

A compact integrated CMOS circuit for temporal differentiation is presented. It consists of a high-gain inverting amplifier, an active non-linear transconductance and a capacitor and requires only 4 transistors in its minimal configuration. The circuit provides two rectified current outputs that are proportional to the temporal derivative of the input voltage signal. Besides the compactness of its design, the presented circuit is not dependent on the DC-value of the input signal, as compared with known integrated differentiator circuits [1]. Measured chip results show that the circuit operates on a large input frequency range for which it provides near-ideal temporal differentiation. The circuit is particularly suited for focal-plane implementations of gradient-based visual motion systems.

1. MOTIVATION

A critical constraint in focal-plane design is the compactness of the pixel. Implementations of gradient-based motion estimation algorithms critically rely on the robust and exact estimation of spatio-temporal intensity gradients [2, 3, 4]. In elaborate 2D motion processing systems, the extraction of the temporal intensity gradient is only a fraction of the total signal processing performed in each pixel [5]. Compact circuits are favorable in order to reduce pixel sizes.

A linear capacitor C is an ideal differentiator because the capacitive current I_c induced by a change in the voltage V_c across the capacitor C is given by

$$I_c = C\frac{dV_c}{dt}.$$

High-gain amplifier feedback circuits have been proposed where the linear resistance R allows an indirect measure of I_c (see *e.g.* [6, 7, 8]).

The "grounded-capacitor" differentiator (Figure 1a) forces the potential V_c on the capacitive node to follow the input signal V_{in}. The voltage V_{out} therefore represents a superposition of the input signal and its temporal derivative which is evident from the circuit's transfer function

$$H_a(s) = \frac{1+\tau s}{1+A^{-1}(1+\tau s)} \approx 1+\tau s \qquad (1)$$

where A is the gain of the amplifier and the approximation is valid for $A \gg 1$.

The "clamped-capacitor" differentiator (Figure 1b) however, clamps V_c to the reference V_{ref}. The voltage V_{out} is now (negatively) proportional to the temporal derivative of the input signal as expressed by the transfer-function

$$H_b(s) = -\frac{\tau s}{1+A^{-1}(1+\tau s)} \approx -\tau s\ . \qquad (2)$$

In both circuits, I_c represents the ideal temporal derivative of the input signal V_{in} for ideal amplification and linear R and C.

Implementations of the two circuits in standard CMOS technology suffer from the limited possibilities to create high linear resistances. Using active resistive elements, implementations of the "grounded-capacitor" differentiator have been proposed such as the "hysteretic differentiator" and the "diff2" circuit [1]. Due to the non-linear characteristics of

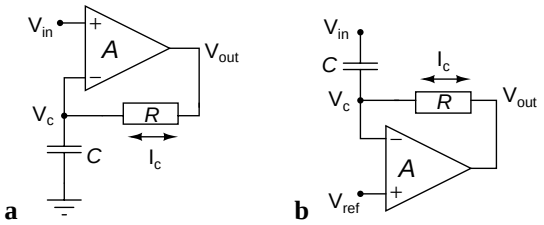

Figure 1: *Two complementary versions of the transconductance amplifier differentiator.* (a) The "grounded-capacitor" differentiator. The voltage V_c is forced to follow V_{in}. (b) The "clamped-capacitor" differentiator. Instead of following the input, V_c is clamped to the reference V_{ref}.

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the resistive elements, the voltage output V_{out} of such implementations shows additional non-idealities besides the inherent superposition property (1). The current I_c, however, still reflects the temporal derivative of the input signal as long as R is sufficiently small not to clip I_c at the output limits of the amplifier. An expansive transconductance element has been suggested that allows to measure I_c and provides two rectified output currents, representing the positive and negative temporal derivative of V_{in} [9]. Such circuit needs a differential transconductance amplifier and consists of at least 7 transistors. It works sufficiently well and has been applied in many gradient-based motion pixel designs [3, 4, 5].

Very few attempts to implement "clamped-capacitor" differentiators have been reported. Moini *etal.* [10] present results of a circuit using a parallel combination of three nonlinear resistive elements. Liu [11] uses a single transistor resistive element where its gate voltage is controlled by the output voltage V_{out} via a source-follower circuit. Both implementations are less compact than the here presented circuit and do not provide a measure of I_c, thus cannot be used as accurate differentiators.

Other implementations that do not directly belong to one of the above feedback amplifier schemes have been suggested, but will not be discussed here.

2. CIRCUIT ARCHITECTURE

I propose a "clamped-capacitor" differentiator circuit that is shown in Figure 2. It consists of an expansive transconductance element formed by a common-source complementary transistor pair [9] and a two-transistor inverting amplifier. The amplifier output V_{out} controls the common gate of the transistor pair in a negative feedback loop in order to clamp voltage V_c at some constant voltage determined by the bias V_{b1}. Ideally, the rectified output currents I^+ and I^- are then proportional to the temporal derivative of the input voltage signal V_{in}.

For saturated sub-threshold operation, neglecting parasitics (for the moment) and transistor sizes and assuming a single constant κ, we can characterize the circuit by

$$I_c = I^+ - I^- = C\frac{d}{dt}(V_{in} - V_c) \quad (3)$$

$$I^+ = I_0 \exp(U_T^{-1}[\kappa V_{out} - V_c]) \quad (4)$$

$$I^- = I_0 \exp(U_T^{-1}[V_c - \kappa V_{out}]) \quad (5)$$

$$V_{out} = -AV_c + V_0\ , \quad (6)$$

where U_T is the thermal voltage and V_0 is some constant offset. We assume that at any moment current flows only through one branch of the expansive transconductance. Considering the case $I^+ \gg I^-$, we substitute (6) into (4), take

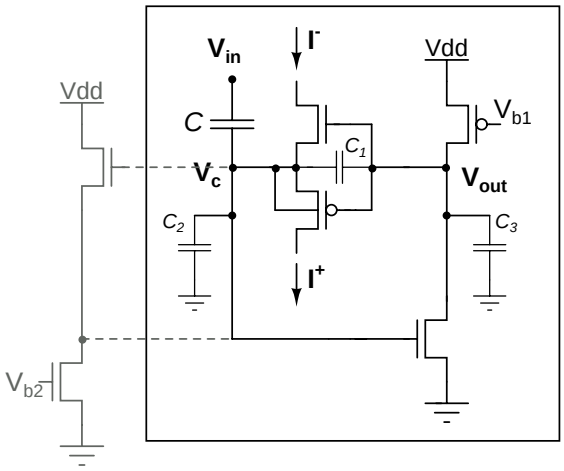

Figure 2: *Circuit Schematics.* C_1, C_2 and C_3 represent inherent parasitic capacitances.

the logarithm and differentiate with respect to time to get

$$\frac{\dot{I}^+}{I^+} = \dot{V}_c(1 + \kappa A)U_T^{-1}\ . \quad (7)$$

Solving (7) for $\dot{V}_c$ and substituting into (3) gives

$$\dot{V}_{in} = \frac{U_T}{2(1+\kappa A)}\frac{\dot{I}^+}{I^+} + \frac{1}{C}I^+. \quad (8)$$

Equation (8) can be integrated for any continuous $V_{in}(t)$,

$$I^+(t) = \frac{1}{\exp(-aV_{in}(t))\left(\frac{a}{C}\int \exp(aV_{in}(t))dt + c_0\right)} \quad (9)$$

where $a = 2(1 + \kappa A)U_T^{-1}$ and c_0 depends on the initial conditions[1].

For linear input $V_{in}(t) = m_0 t + c_1$ with $m_0 > 0$, the output current (9) simplifies to

$$I^+(t) = \frac{Cm_0}{1 + c_0 Cm_0 \exp[-2m_0 t(\kappa A + 1)U_T^{-1} + c_1]}. \quad (10)$$

We note that the circuit exponentially approximates an ideal differentiator for linear input. The time-constant is directly dependent on the amplifier gain A, with

$$A = \frac{g_m}{g_o} = \frac{\kappa}{U_T}\left(\frac{V_{En}V_{Ep}}{V_{En} + V_{Ep}}\right) \quad (11)$$

where V_{En}, V_{Ep} are the Early-voltages. Clearly, high gain improves the approximation of ideal differentiation.

The *small signal regime* of the circuit is determined by the finite gain A of the amplifier, the characteristics of the

[1]The analysis for $I^- \gg I^+$ is equivalent and not shown here.

expansive transconductance element and the parasitic capacitances. For small input amplitudes ΔV_{in}, the change $\Delta(V_{out} - V_c)$ will be small and remain within the high resistance regime of the expansive transconductance element (see Figure 5). This approximately leads to open-loop conditions where $I^+, I_- \approx 0$. Considering the parasitic capacitances (C_1, C_2 and C_3 in Figure 2), a change in the input ΔV_{in} will then result in a change of the capacitive node

$$\Delta V_c = \frac{C}{C + C_1(1+A) + C_2} \Delta V_{in}$$

thus V_c is not clamped and follows V_{in}. The gate-overlap capacitance C_1 thereby is most effective (through its multiplication with the amplifier gain A) and reduces the total loop gain through capacitive *positive feedback*. This results in an actual increase of the small-signal regime. In any case, C_1 should be minimized because A needs to be large (10).

C_3 limits the bandwidth of the differentiator circuit. According to Figure 2, the time-constant of the amplifier is $\tau = g_o^{-1}(C_1 + C_3)$. Since g_o is proportional to the bias current[2], the cut-off frequency can be increased at the cost of higher power consumption.

Reverse currents of the n-diffusion layers to the bulk such as the source of the nFET and the n-well of the pFET transistor of the expansive transconductance element can affect the circuit behavior significantly. The total leak current to substrate induces *asymmetry* because of the rectified nature of I^+ and I^-. Given

$$I_c = I^+ - I^- + I_{leak} \ ,$$

I_{leak} represents the detection threshold for I^+ and simultaneously also the constant offset of I^-. I_{leak} is not affected by the input signal but strongly depends on the density of minority carriers. A careful management of photo-induced minority carriers is recommended for the use of the circuit in focal-plane arrays.

3. MEASUREMENTS

The circuit has been fabricated in a 0.8 μm CMOS process. The transistors in the amplifier have a size ratio $W/L = 0.5$ and the capacitor has a value of $C = 1.05$ pF. The total silicon area is 1350 μm^2, with the poly-poly capacitor occupying 74% of it. Top and bottom of the transconductance element are connected to current mirrors. After being amplified on-chip, the output currents were measured off-chip by high-speed current-sense amplifier circuits. The current values indicated in the following figures are scaled back to represent the original currents I^+ and I^-.

For testing purposes, the circuit has been slightly modified in order to be able to bias the amplifier independently of the capacitive node potential V_c. A source-follower[3] has been inserted to the feedback loop as shown in Figure 2. Biased always slightly above the inverting amplifier, this additional stage does not affect the circuit behavior significantly besides reducing the feedback gain A by $1/\kappa$.

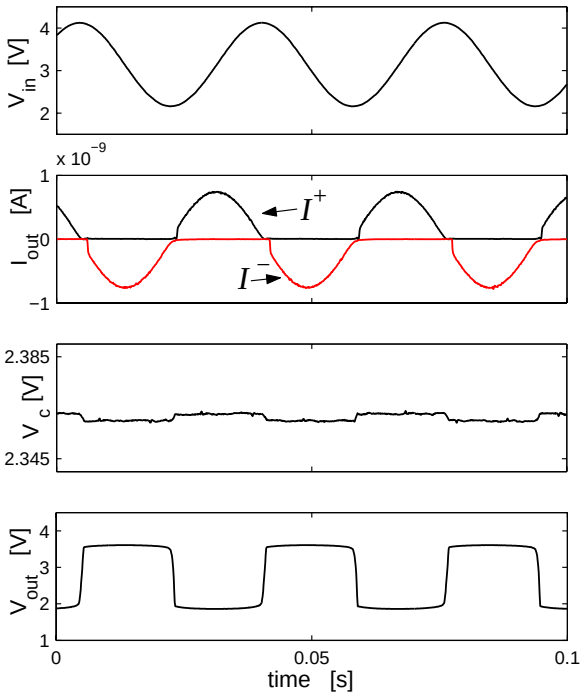

Figure 3: *Circuits characteristics to a sine-wave input signal.* From top to bottom: Input signal V_{in}, rectified output currents I^+ and I^- (gray line), clamped capacitive node V_c (scale!) and the amplifier output voltage V_{out}.

Figure 3 shows the measured voltage and current signals at different stages of the circuit. The output currents I^+, I^- show clear rectification and well approximate temporal differentiation. The small signal behavior is apparent at zero-crossings of the input gradient where V_c slightly follows the input V_{in}. Note the symmetric output responses and the good overall clamping of the capacitive node V_c.

The accuracy of differentiation is shown in Figure 4a where the peak output currents are plotted against the maximal temporal gradient of the sine-wave input signal. Deviation from linearity was $1.9 \pm 1.4\%$ in the measured frequency range. Here, the amplifier was biased above threshold ($V_{b1} = 4$ V) to shift the cutoff-frequency beyond the measurement range. Figure 4b shows the measured cut-off frequency (sine-wave, amplitude 2 V) as a function of the amplifier bias voltage V_{b1}. The semi-logarithmic graph illustrates nicely its relation to the bias current which is linear in the sub-threshold regime and turns into a square-root

[2] $g_o \propto I_{bias}$ in subthreshold; $g_o \propto \sqrt{I_{bias}}$ above threshold

[3] The source-follower *replaces* the direct connection of V_c to the amplifier input. Note, that it is not necessary to guarantee correct operation.

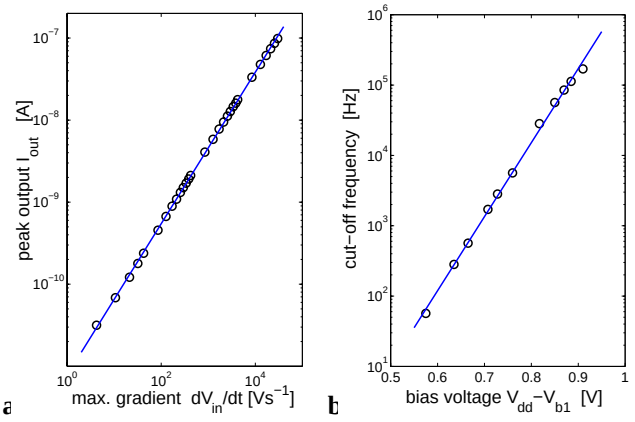

Figure 4: *Linearity and band-width limit (data and fit).* (a) Peak response as a function of maximum input gradient. (b) Cut-off frequencies as a function of the bias voltage V_{b1}.

dependence when passing threshold. It confirms that the operational limits of the circuits are dominated by the time-constant of the amplifier.

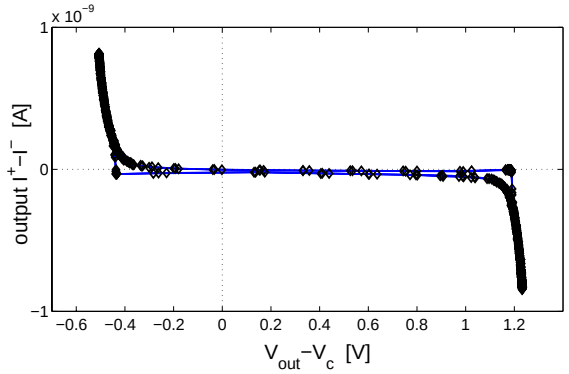

Figure 5: *Characteristics of the expansive transconductance.*

Figure 5 shows the *dynamic* characteristics of the expansive transconductance, extracted from the measurements shown in Figure 3. Due to its exponential behavior, the effective conductance is relatively small for a large fraction of its operational voltage range, dominating the small-signal regime.

The observed hysteresis in Figure 5 is induced by the dynamics of the diode-connected current mirrors[4], necessary for reading out I^+ and I^-. When alternatively turning on or off, the current mirrors show a transient response which is dominated by their parasitic gate-capacitances. Hysteresis results because the time-constant for turning on is shorter than for turning off. The positive current offset at $\Delta V = 0$ represents the total leakage current I_{leak}.

[4]not shown in Figure2.

4. CONCLUSION

I presented and analyzed a circuit for temporal differentiation. The circuit is more compact than any previously proposed integrated architecture of comparable accuracy and power efficiency which makes it particularly suited for focal-plane motion processing arrays. The "clamped-capacitor" arrangement has the advantage of avoiding any DC-dependence of the input signal, thus allowing for accurate differentiation in virtually any input range. Measured chip results confirm the feasibility of the proposed circuit, showing accurate wide-band differentiation for operation in sub-threshold with a cut-off frequency beyond the needs of typical visual temporal processing.

5. ACKNOWLEDGEMENTS

I would like to dedicate this paper to the late Jörg Kramer, who was a true friend and an invaluable colleague.

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