Next-Generation Energy Harvesting Electronics: Holistic Approach
**Workshop and Showcase**
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# Efficient and adaptive power electronics for Energy Harvesting

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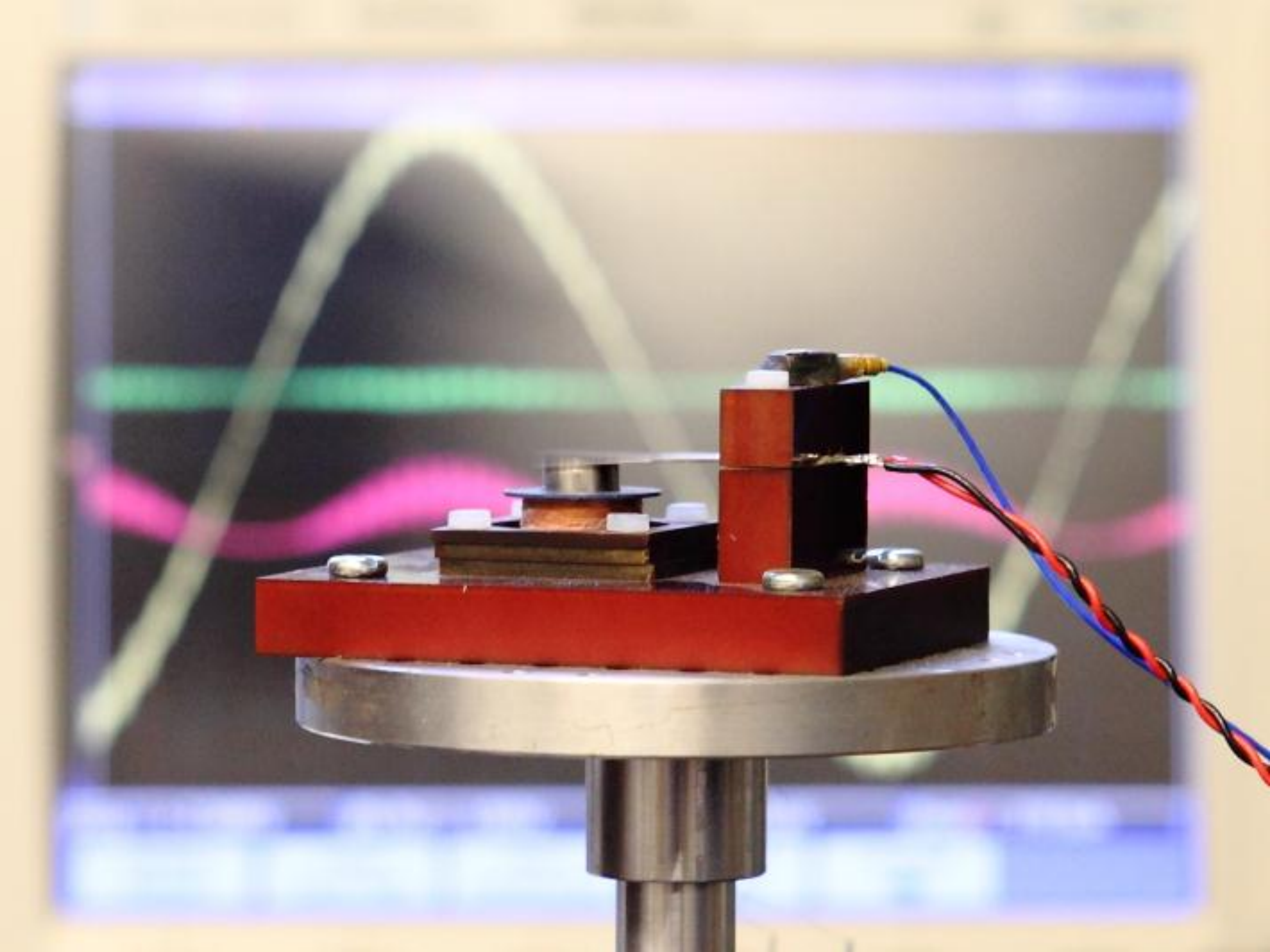
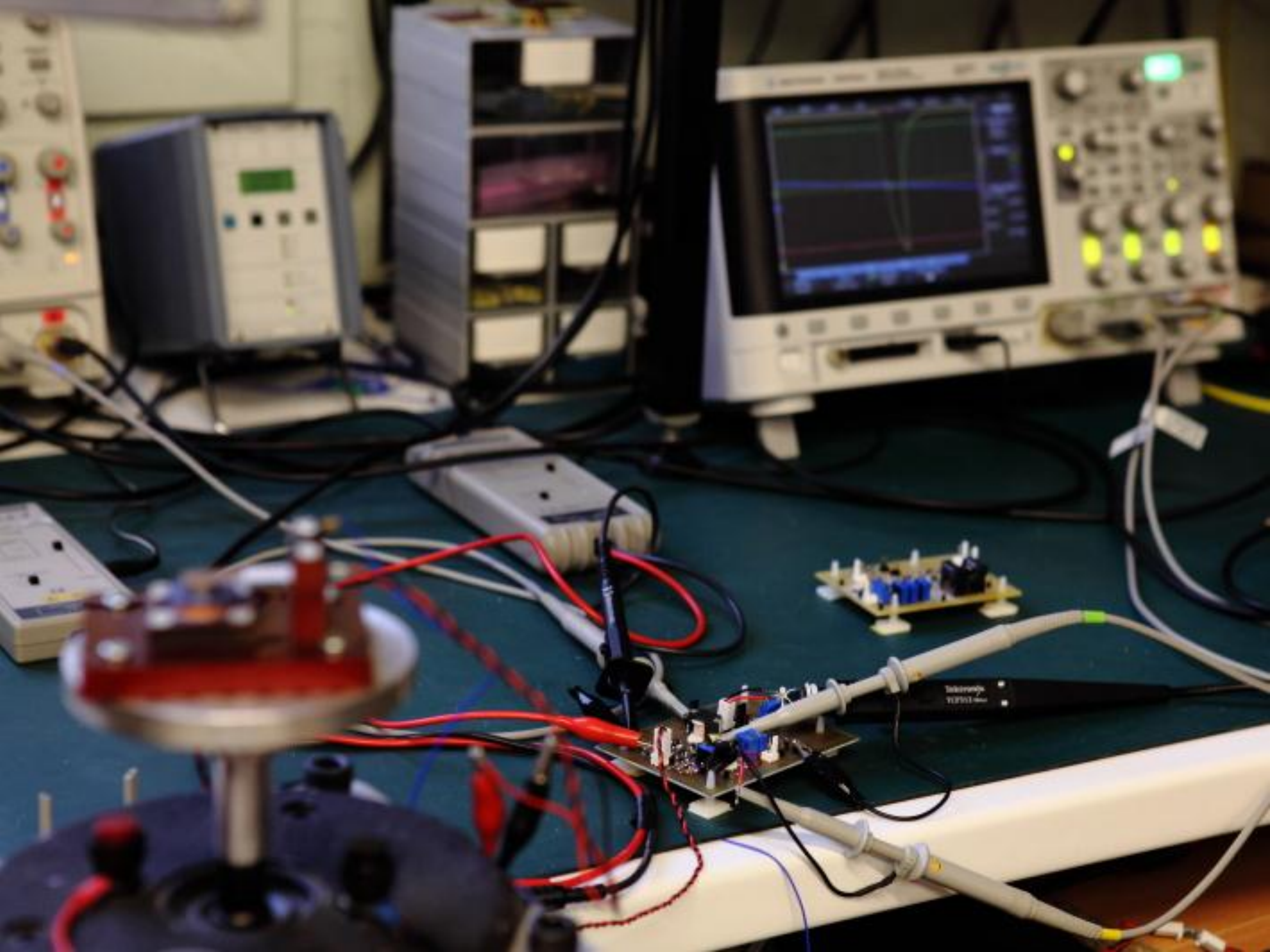
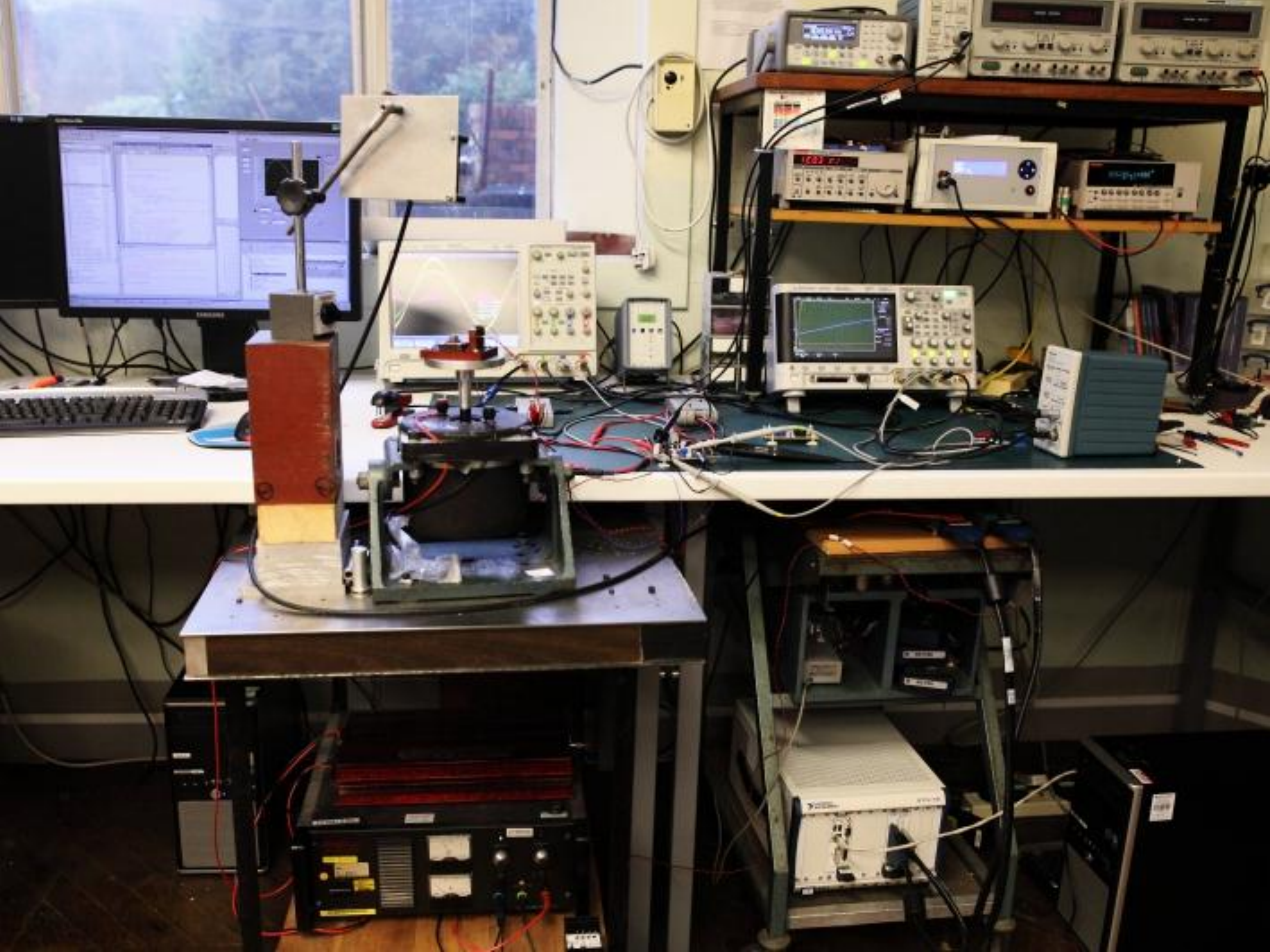
University of BRISTOL

*Electrical Energy Management Research Group*

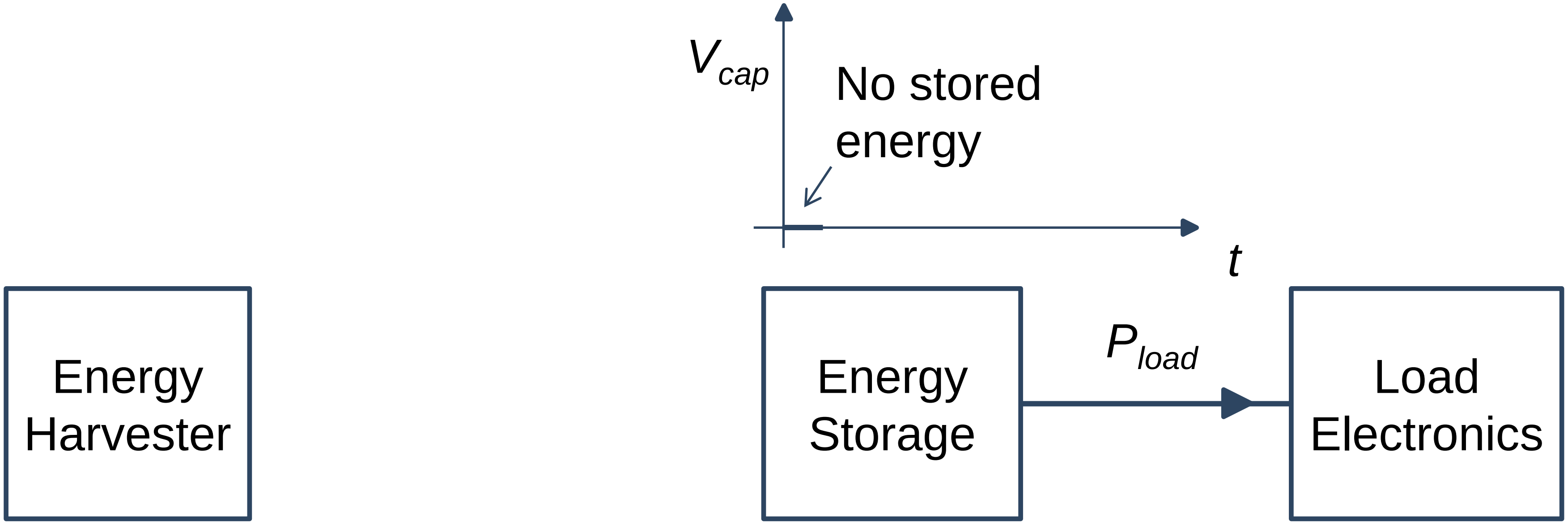
holistic energy harvesting




Tektronix



# System operation from cold start



$V_{cap}$

No stored energy

$t$

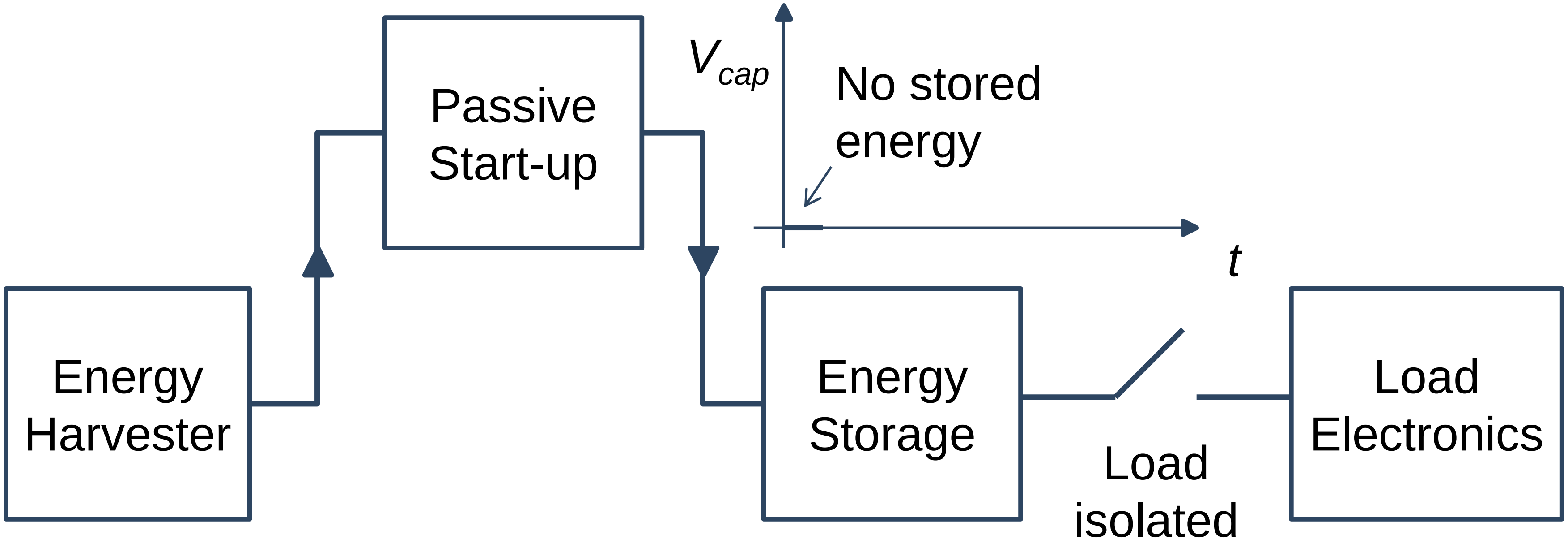
Energy Harvester

Energy Storage

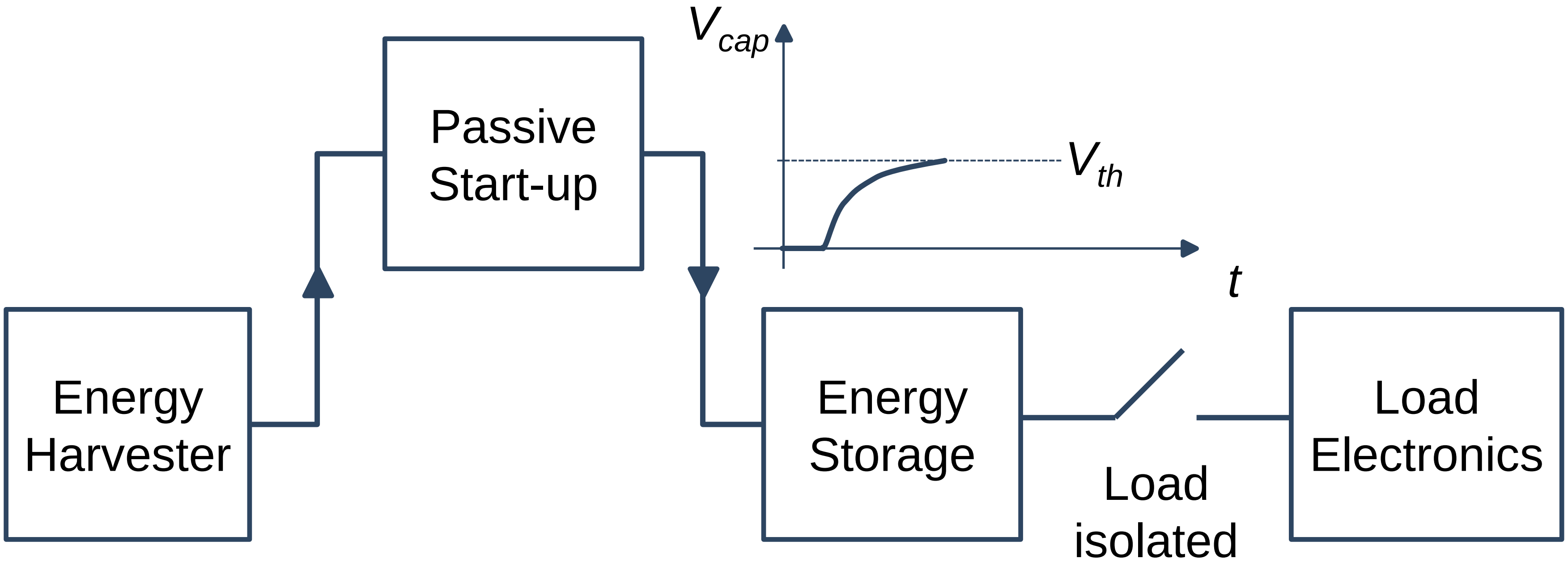
$P_{load}$

Load Electronics

# System operation from cold start



# System operation from cold start



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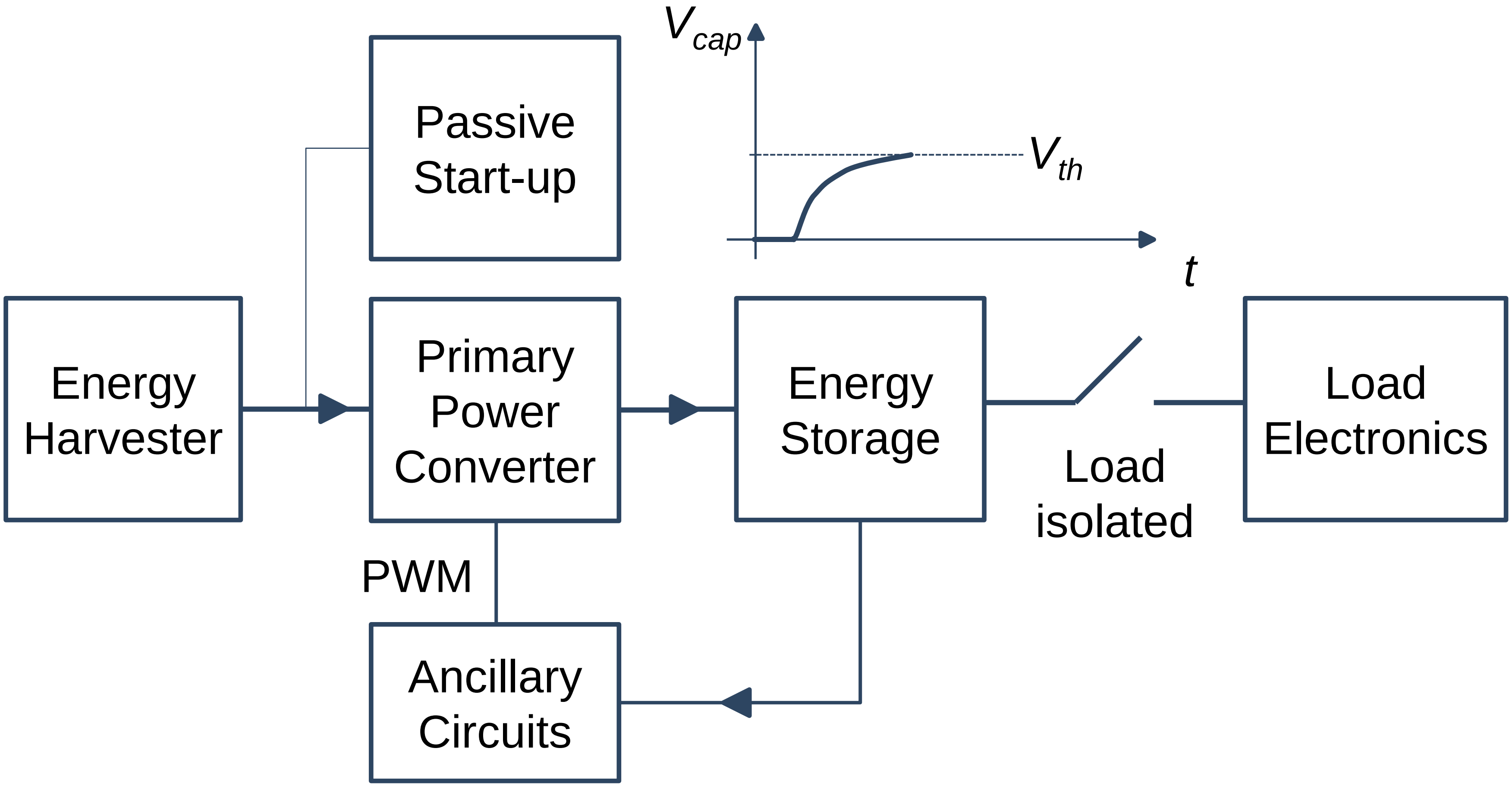
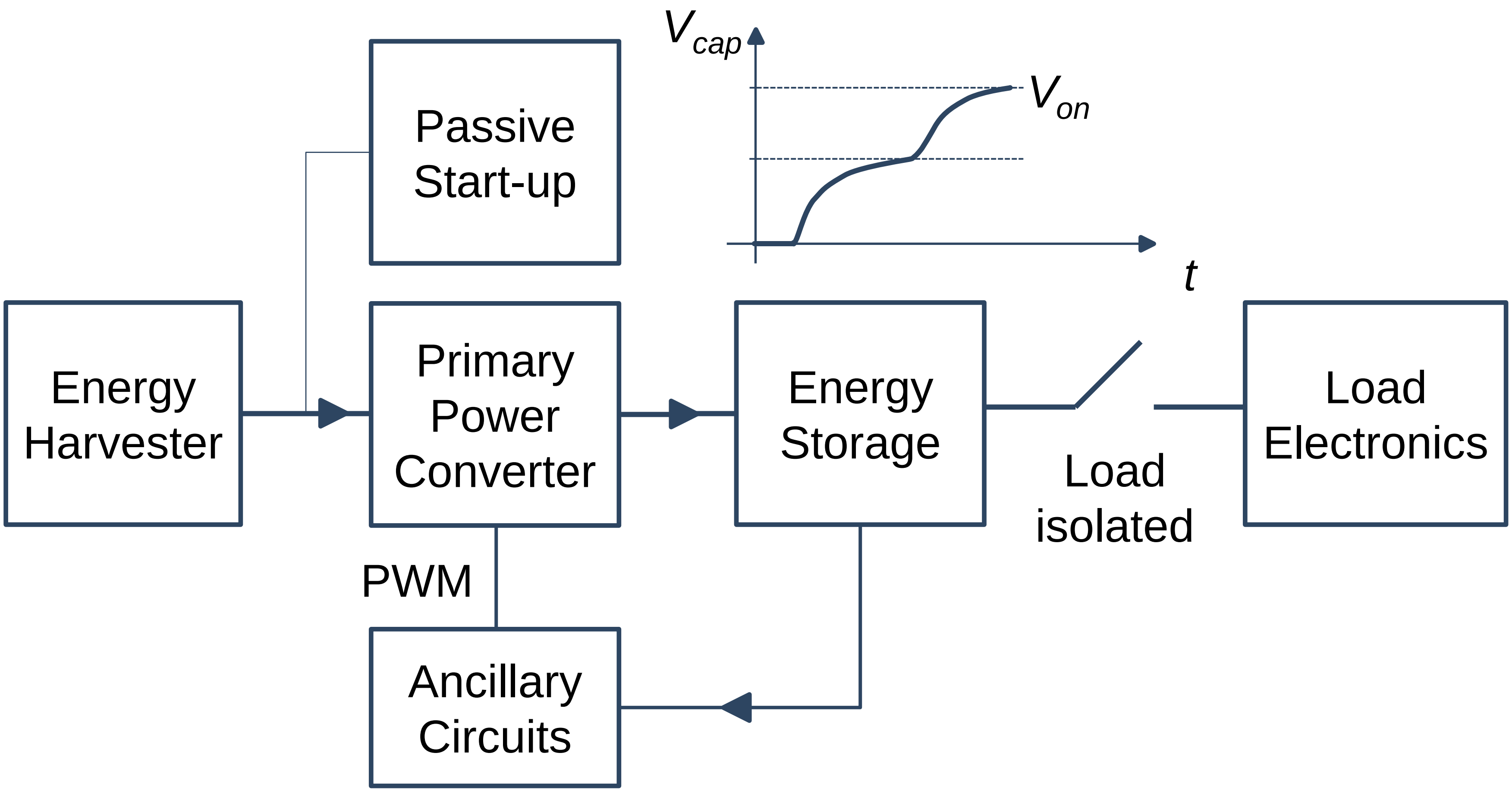
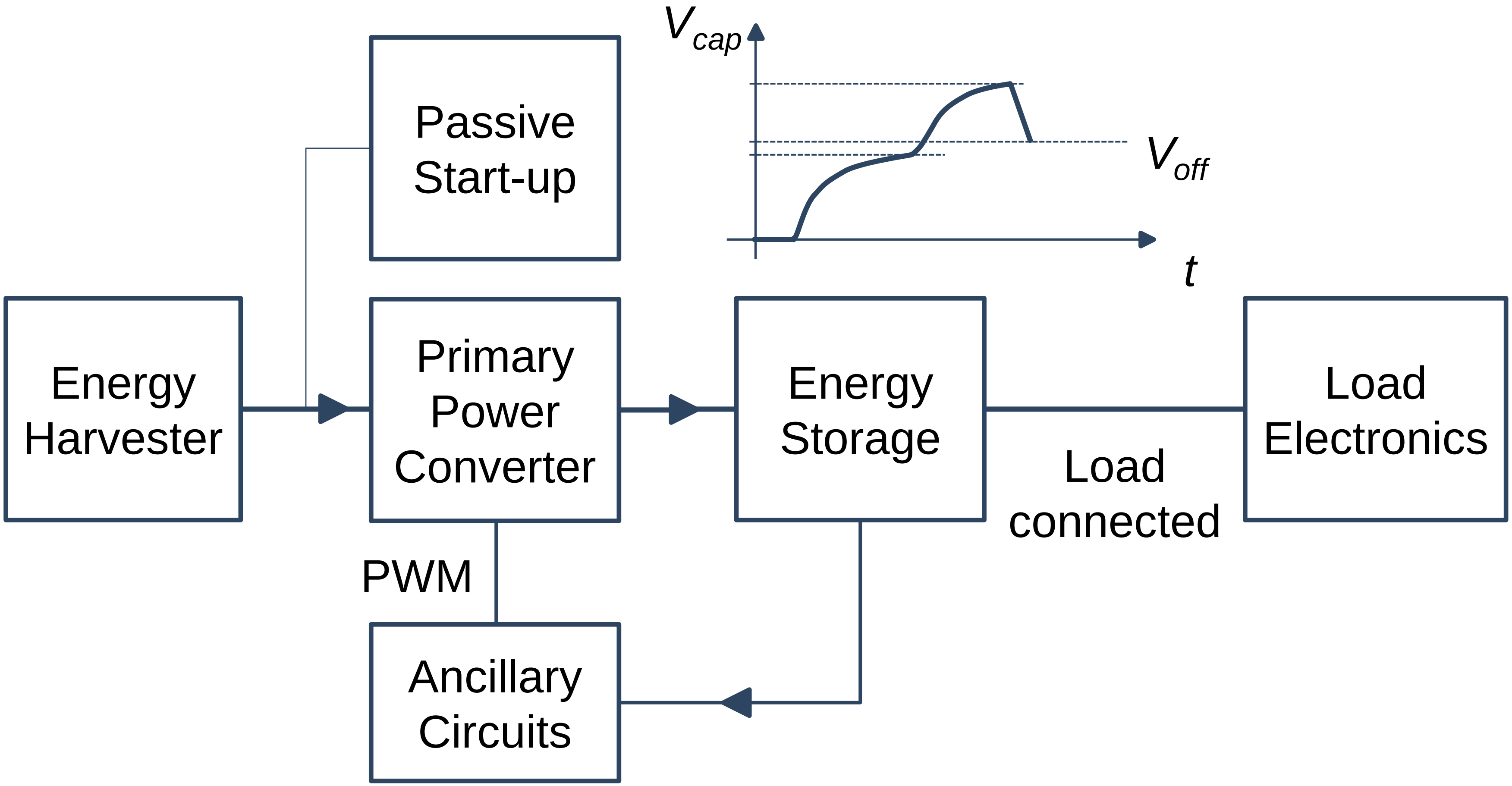


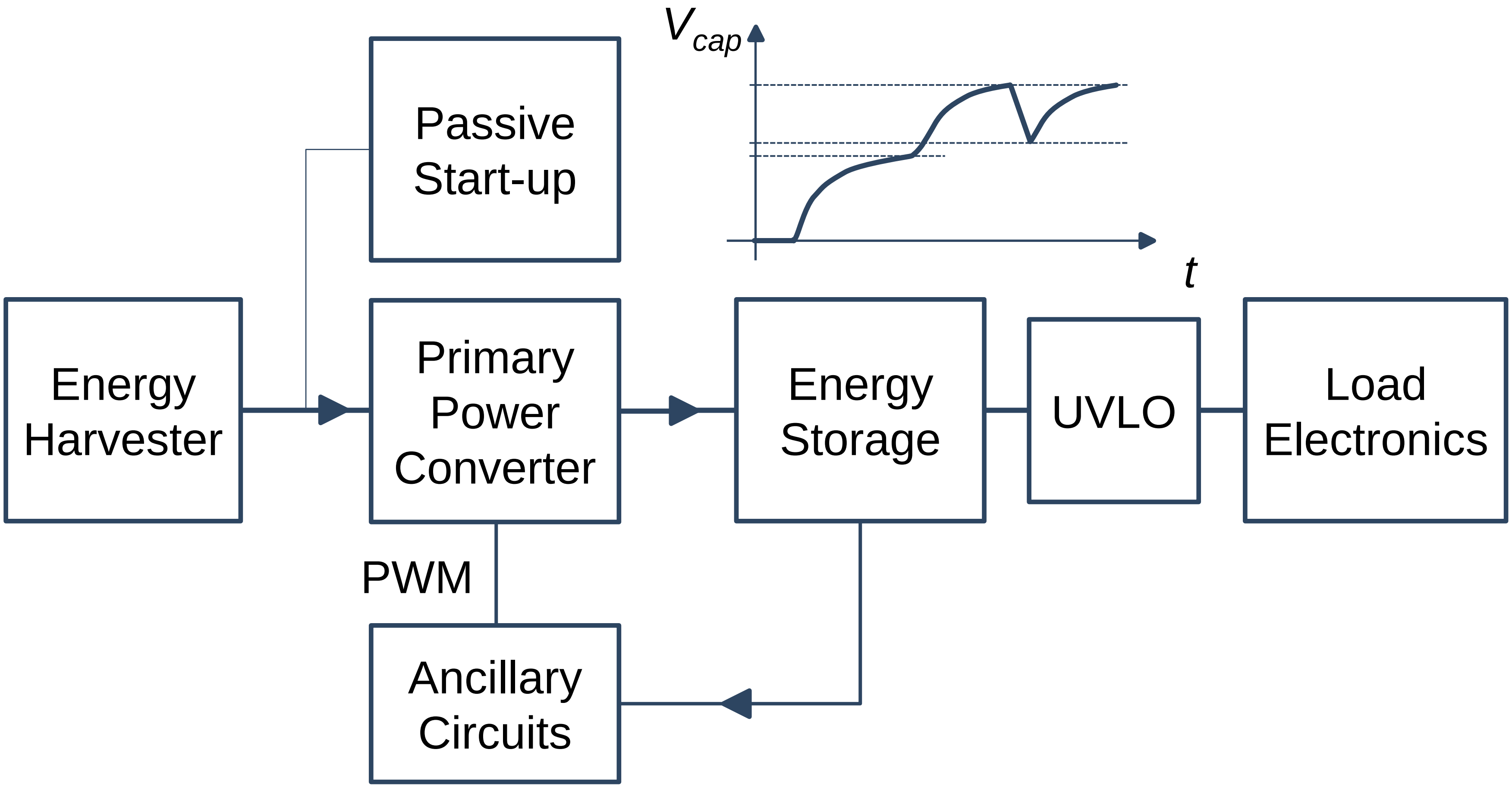
# System operation from cold start



# System operation from cold start



# System operation from cold start

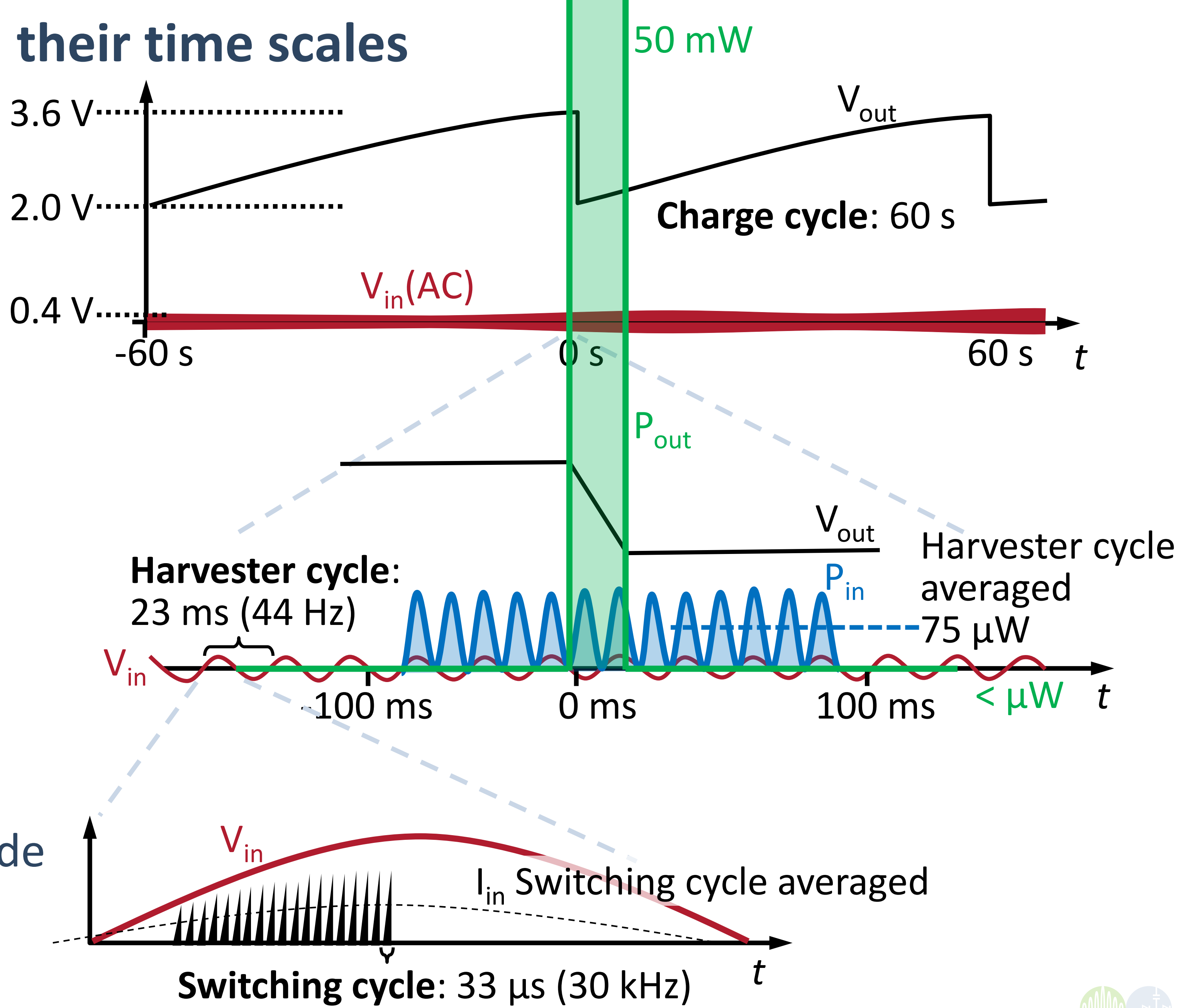


# 3 cycles and their time scales

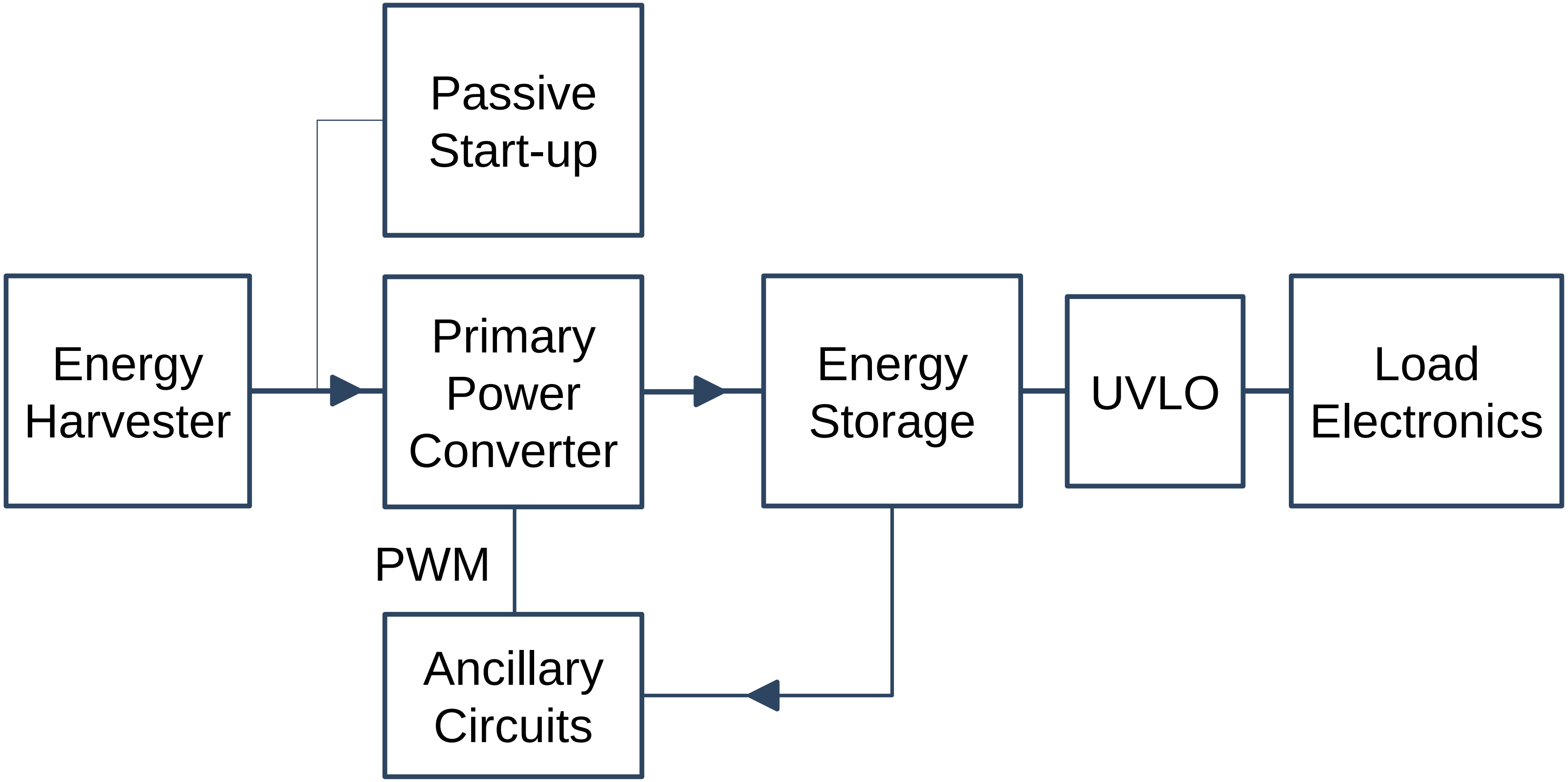
Voltage boosting ×10

Power boosting ×1000

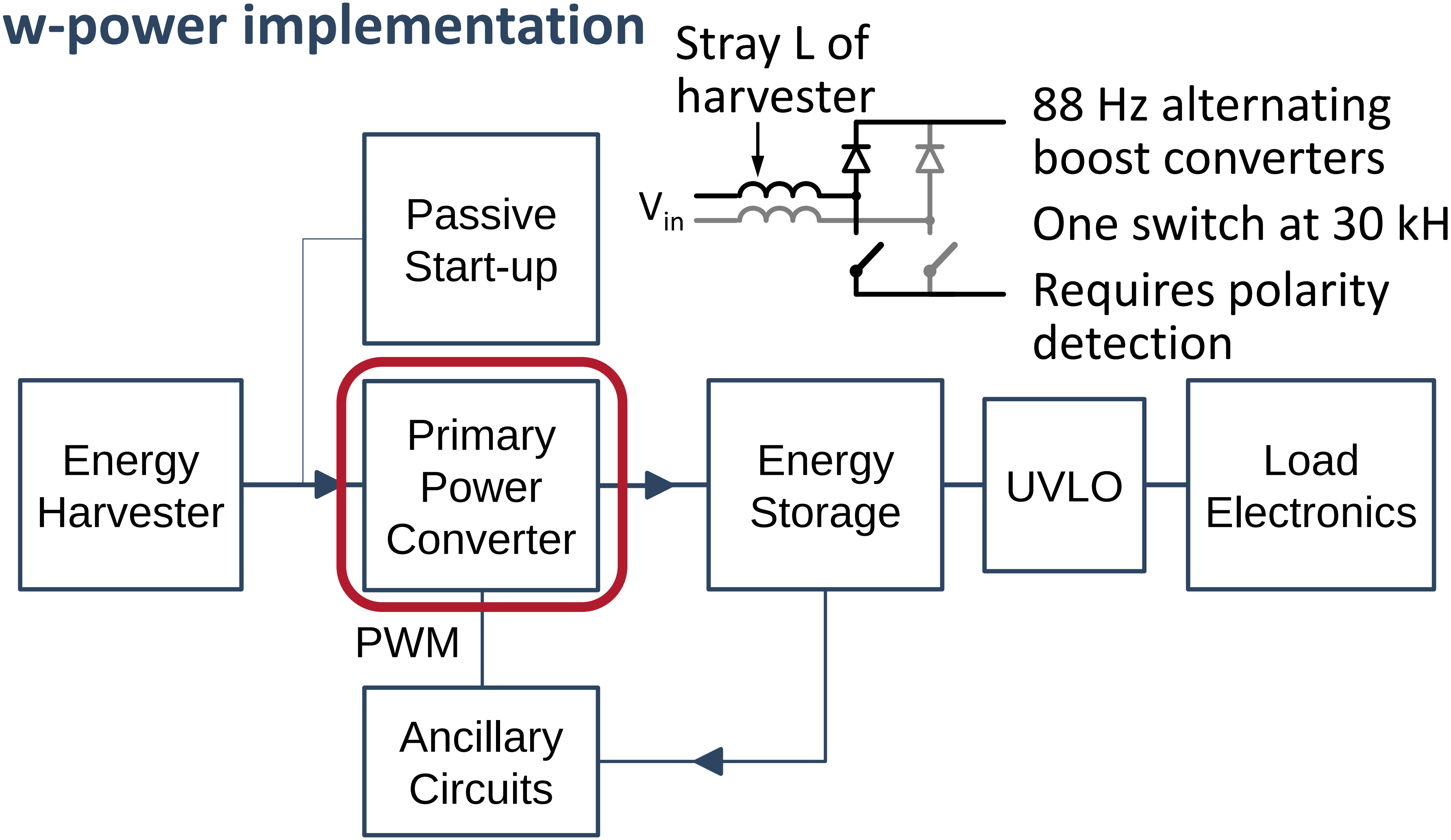
Switched–mode conversion



# Low-power implementation



# Low-power implementation

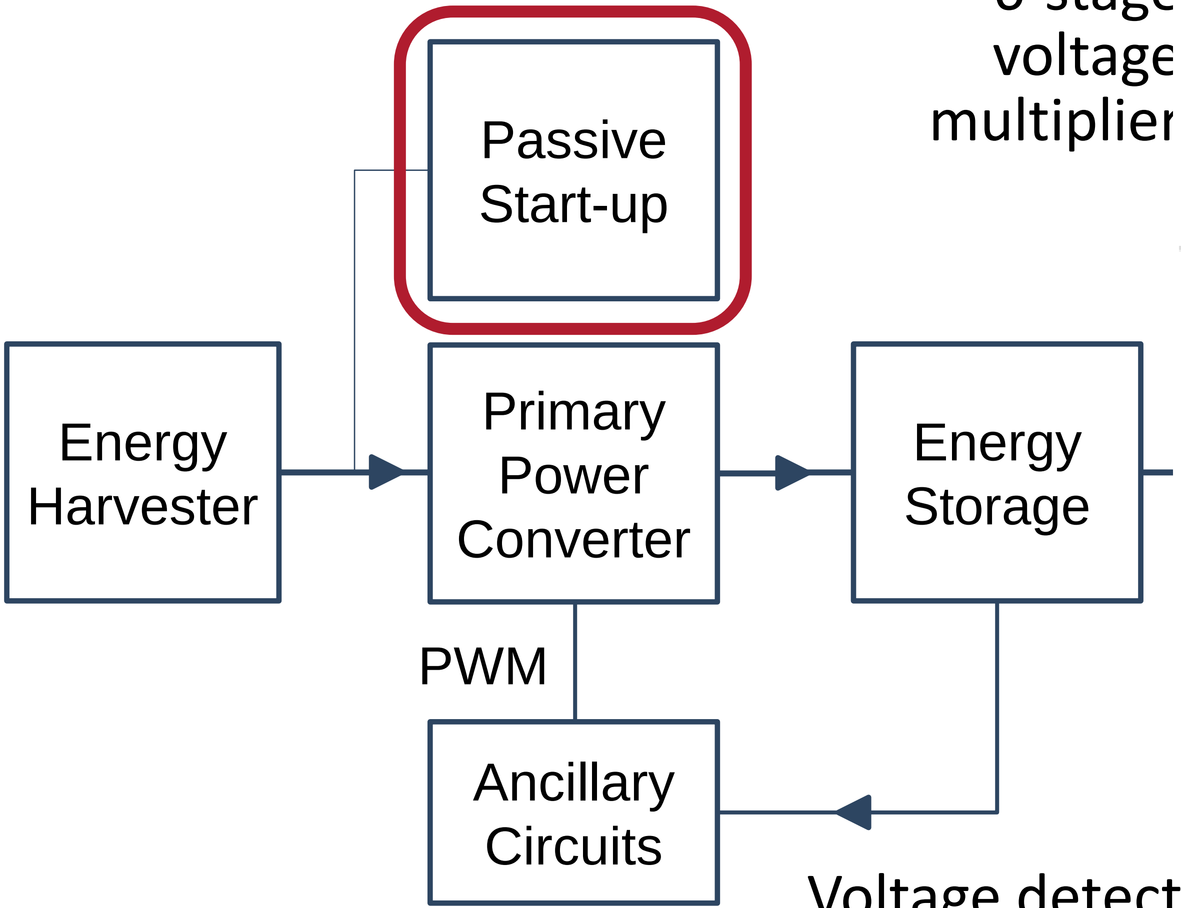


88 Hz alternating boost converters

One switch at 30 kHz

Requires polarity detection

# Low-power implementation



Passive Start-up

Energy Harvester

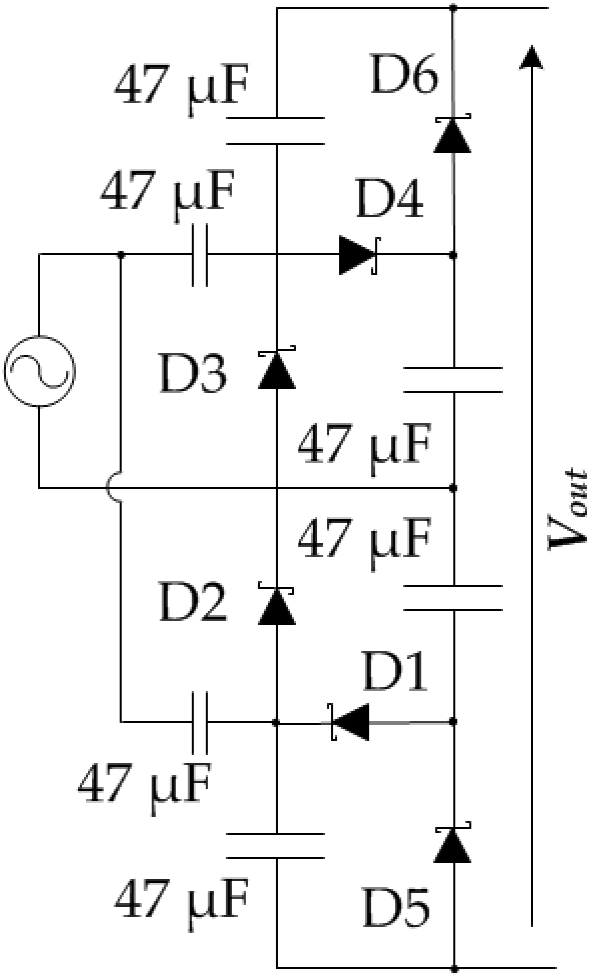
Primary Power Converter

Energy Storage

PWM

Ancillary Circuits

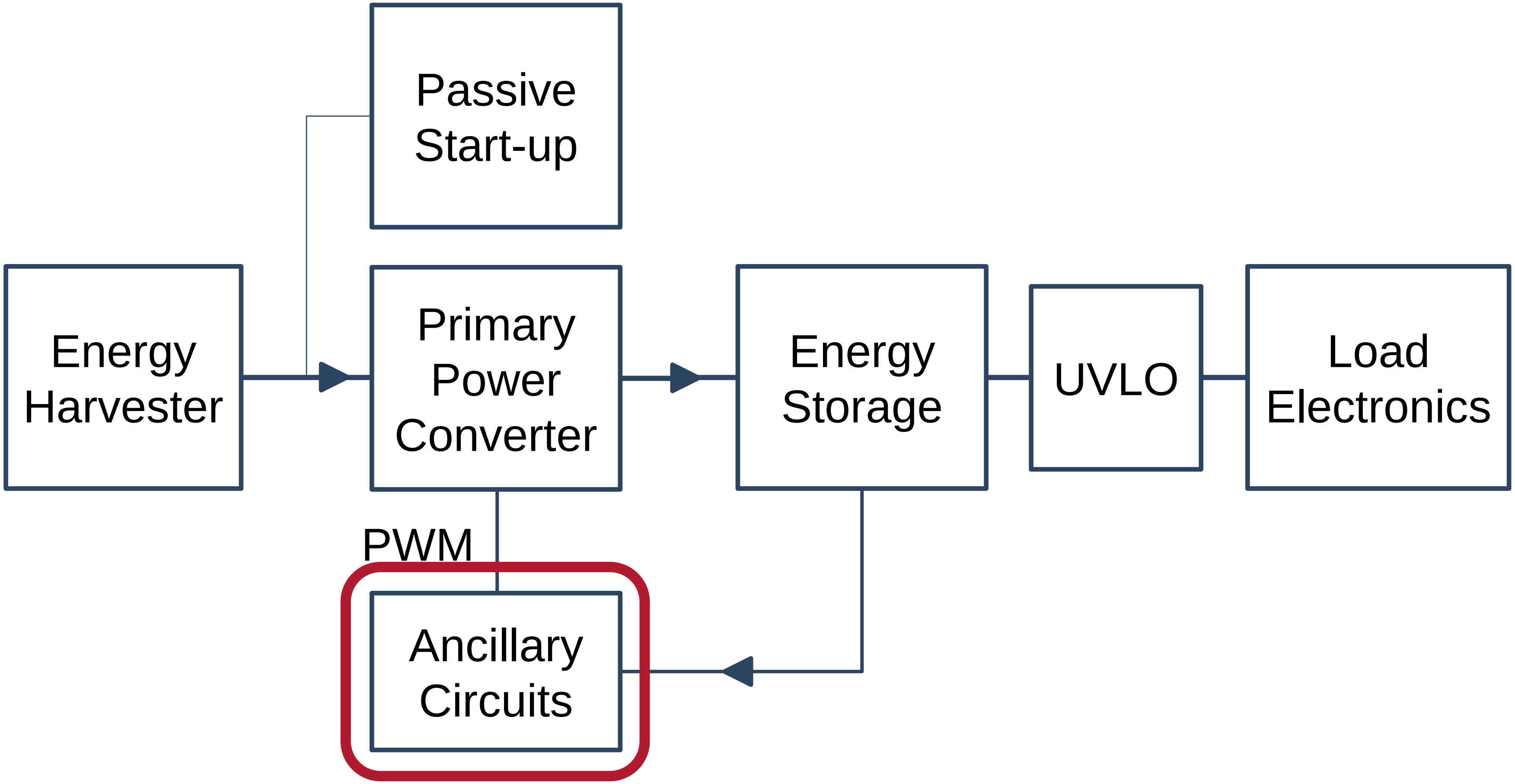
6-stage voltage multiplier



Voltage detector power-gates the µC

µC controls activation of ancillary circuits and isolates voltage multiplier via JFET isolation switches

# Low-power implementation

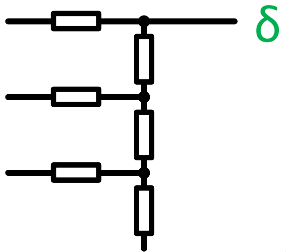


# Low power implementations: useful ancillary circuits

**DAC**

µC outputs active in low-power mode

R2R matrix



**PWM**

Quartz osc.

FF

Precision RC + comparator

Jitter < 0.2%
max δ = 97%

**µC** LPM4 = 100 nA
max clock frequency

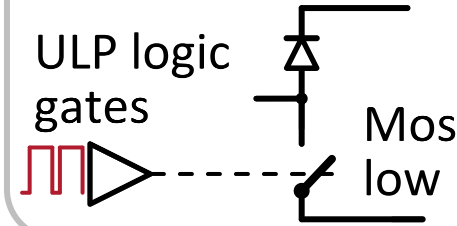
on once per 23 ms
harvester cycle for 4 µs

on once every 15 harvester cycles for 34 µs to track max power transfer:

measure $I_{out}$, calculate direction, perturb δ

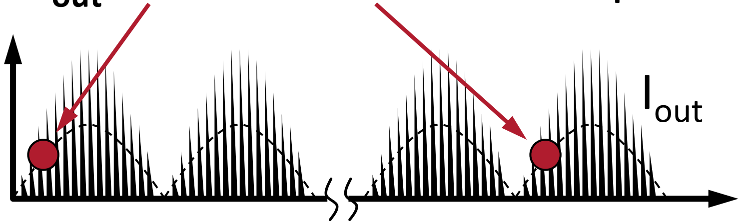
**Gate drive**

ULP logic gates



Mosfets selected for low $R_{DS(on)}$ and $Q_{GS}$

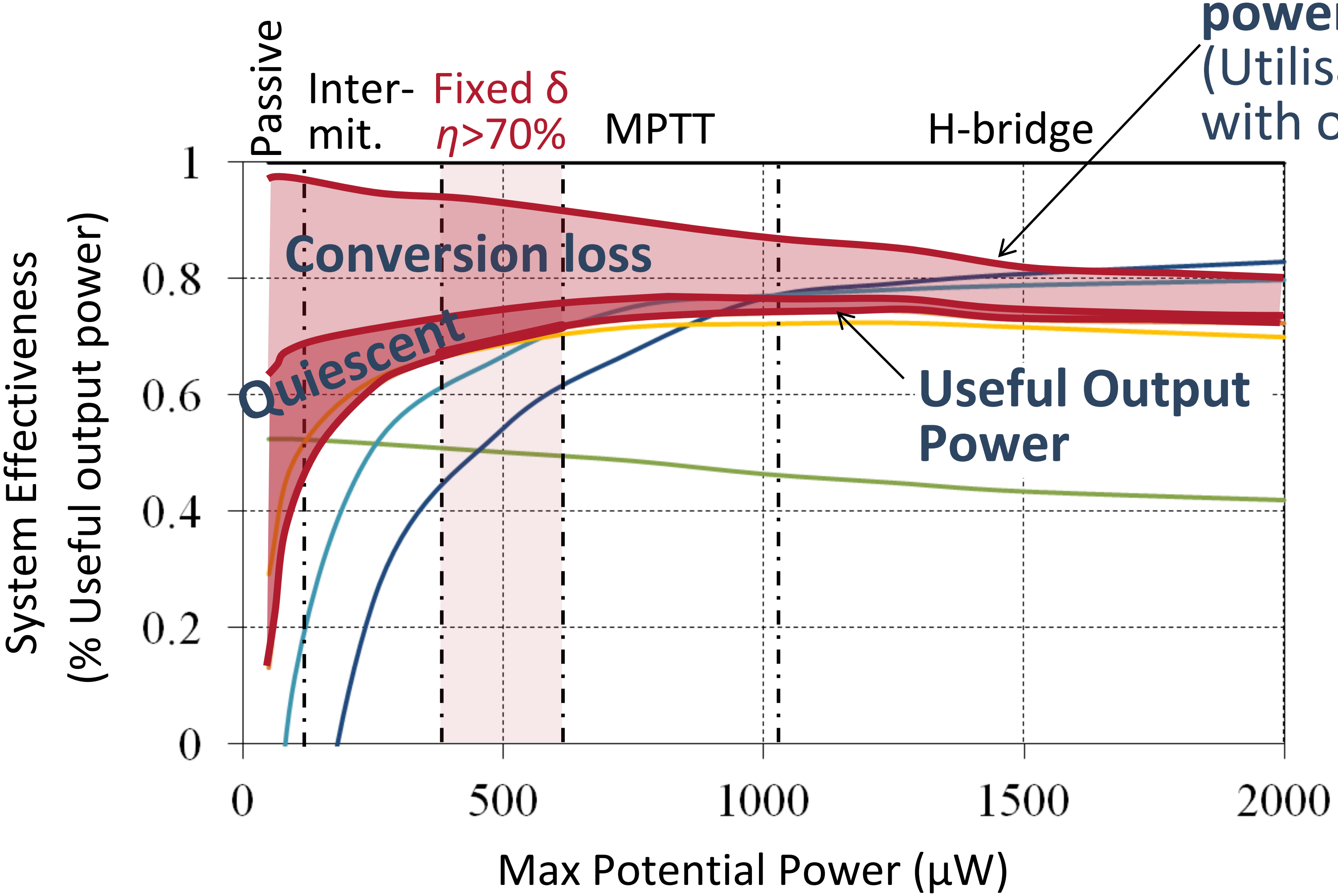
$\Delta I_{out}$ **measurement** for max power transfer tracking



Synchronised to harvester cycle

12 Hz low-pass filter: Low power OpAmp continuously on to avoid settling time

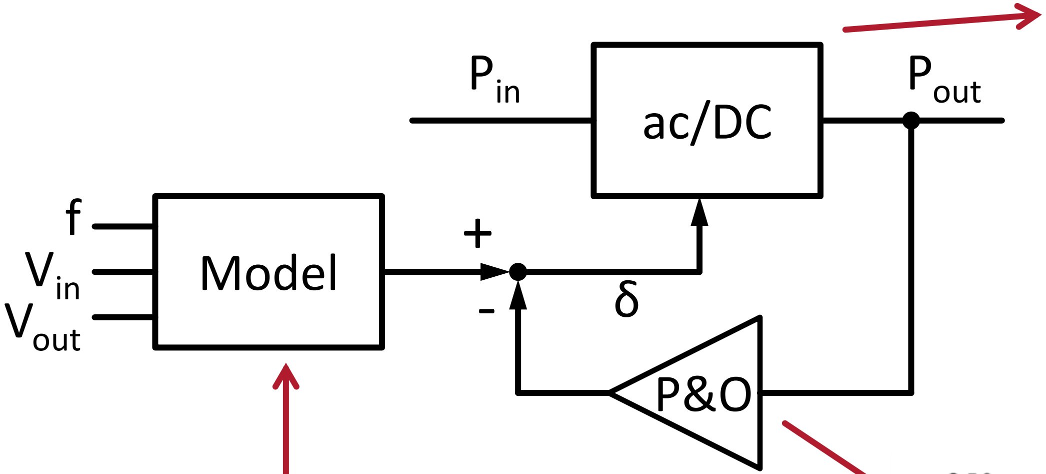
# Comparing control techniques

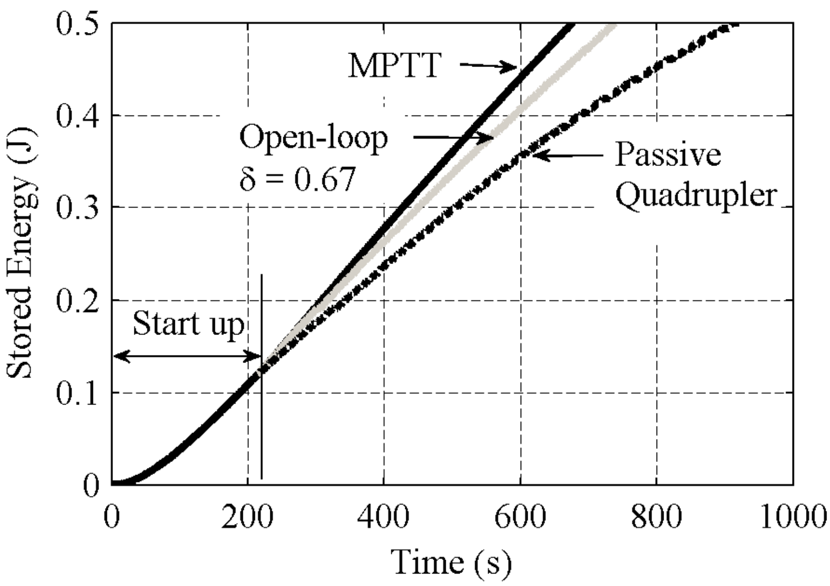


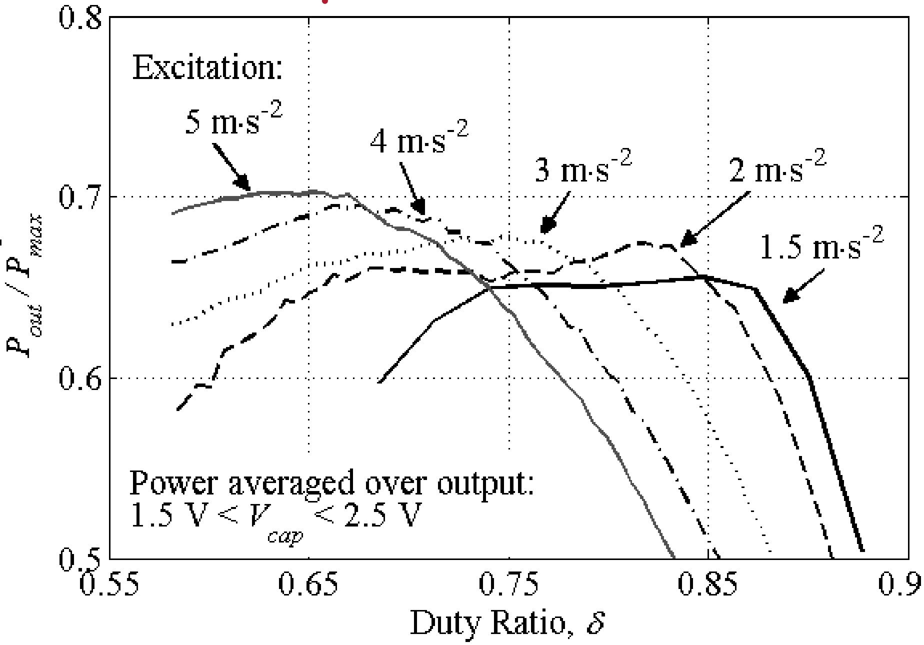
**Harvester output power**
(Utilisation drops with output power)

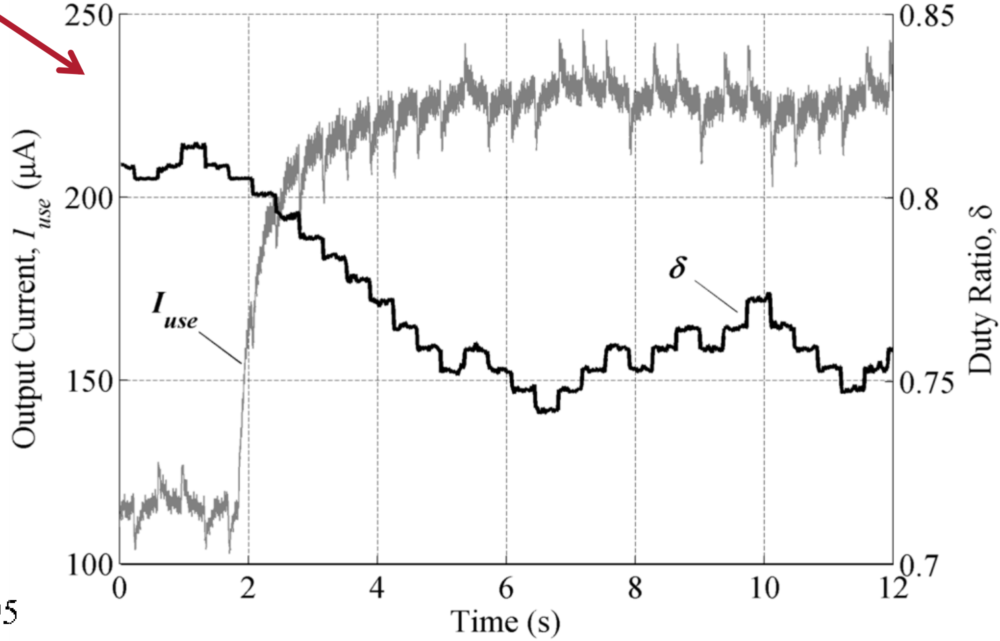
**Useful Output Power**

# Options for adaptation

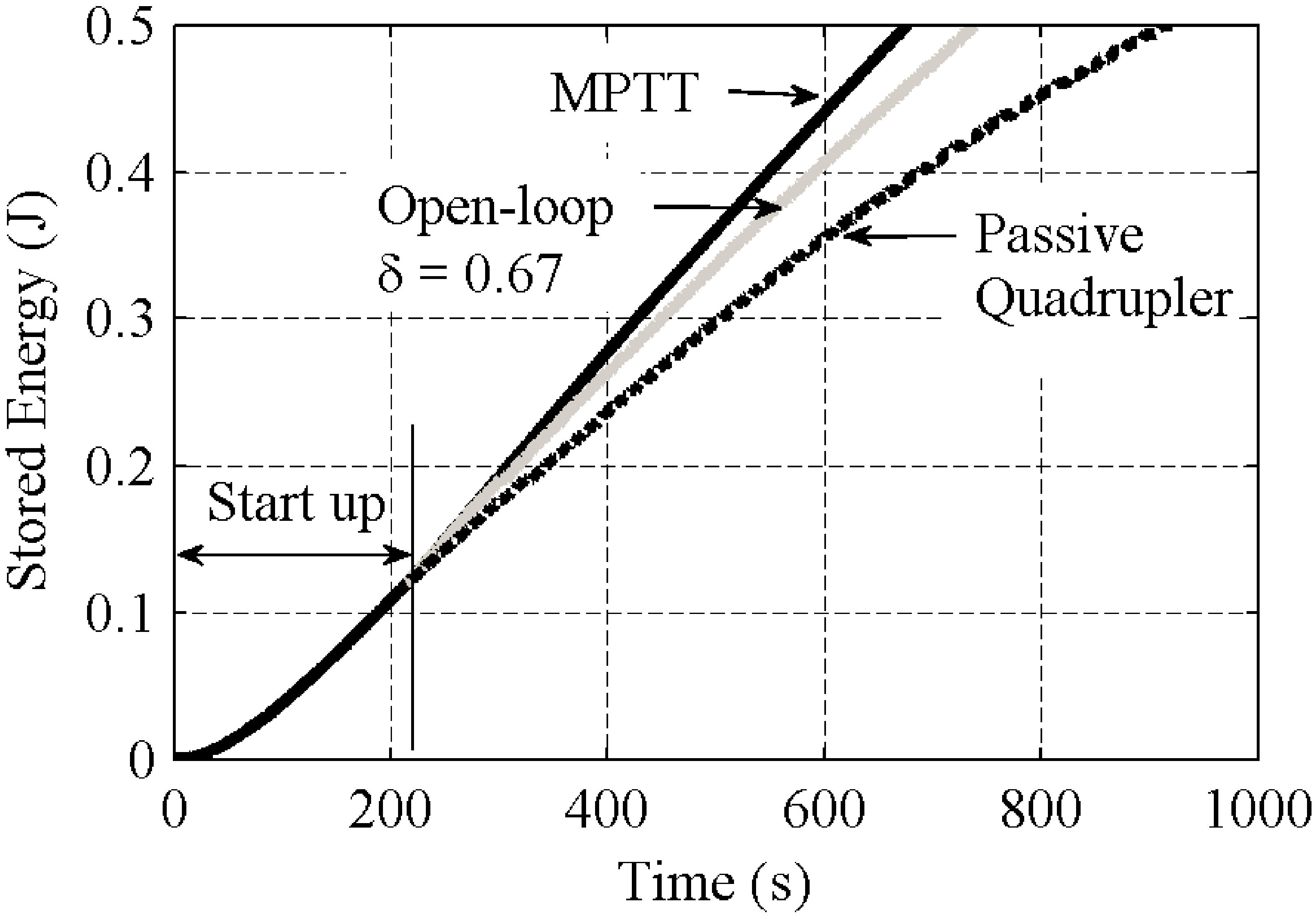


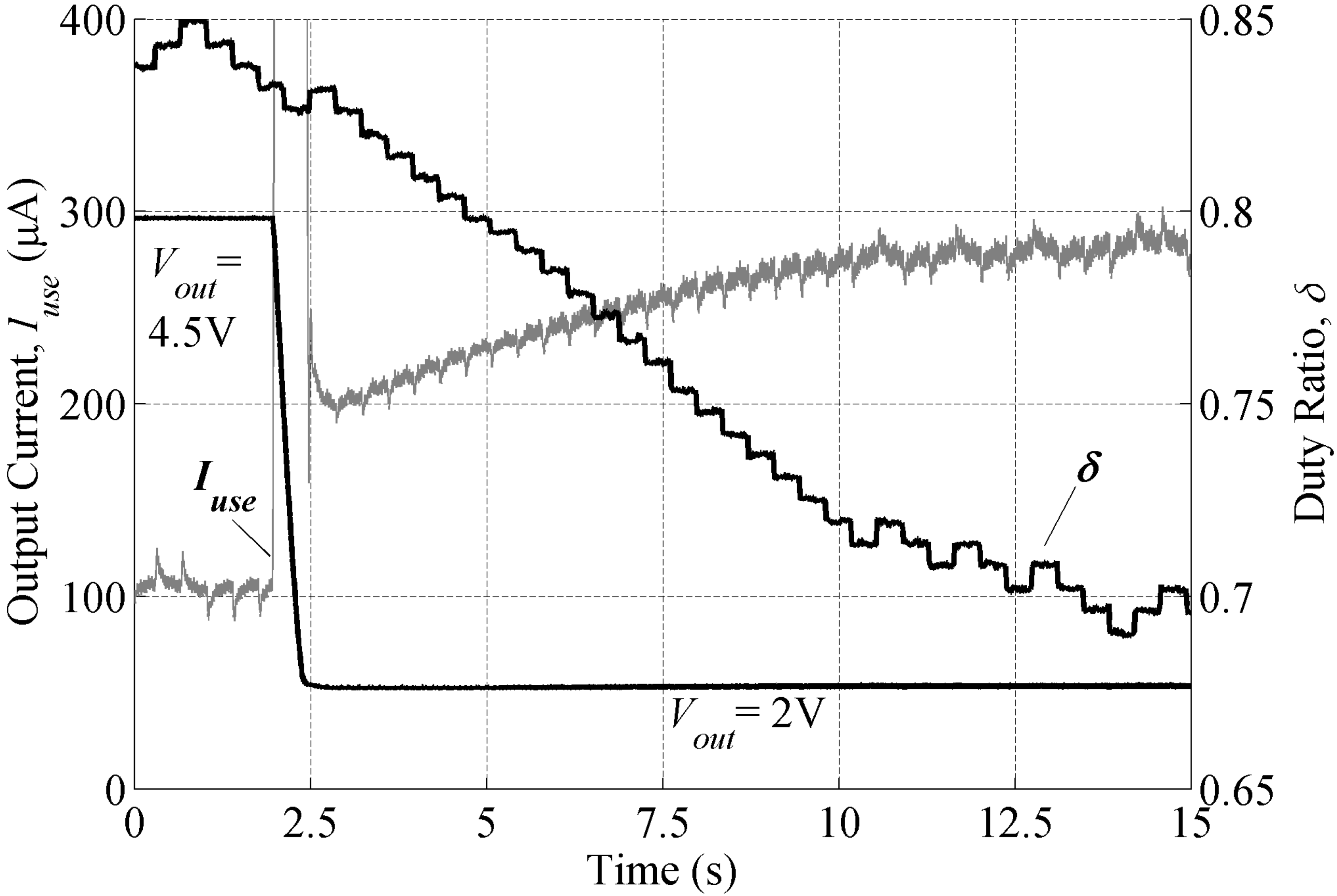


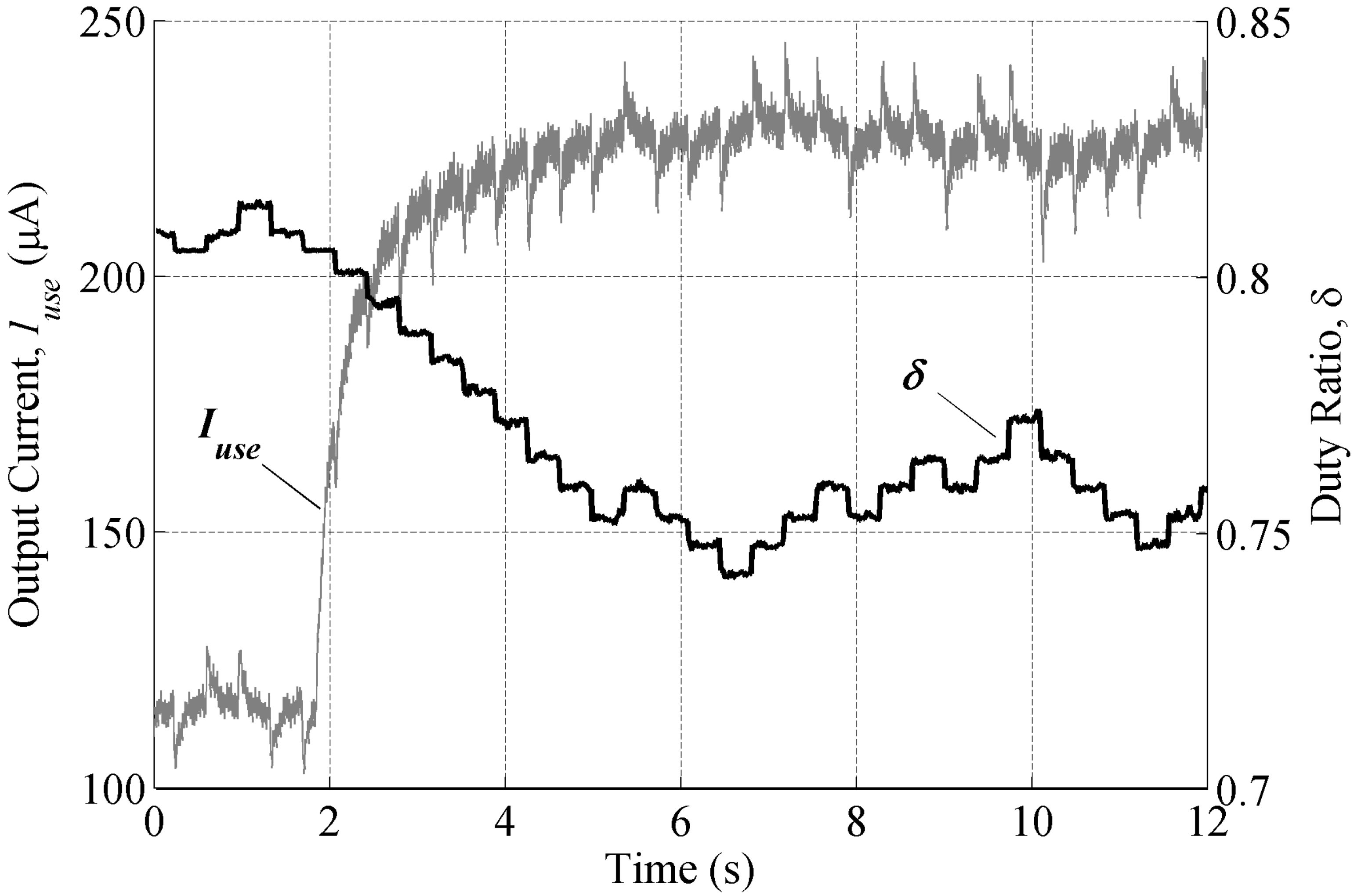


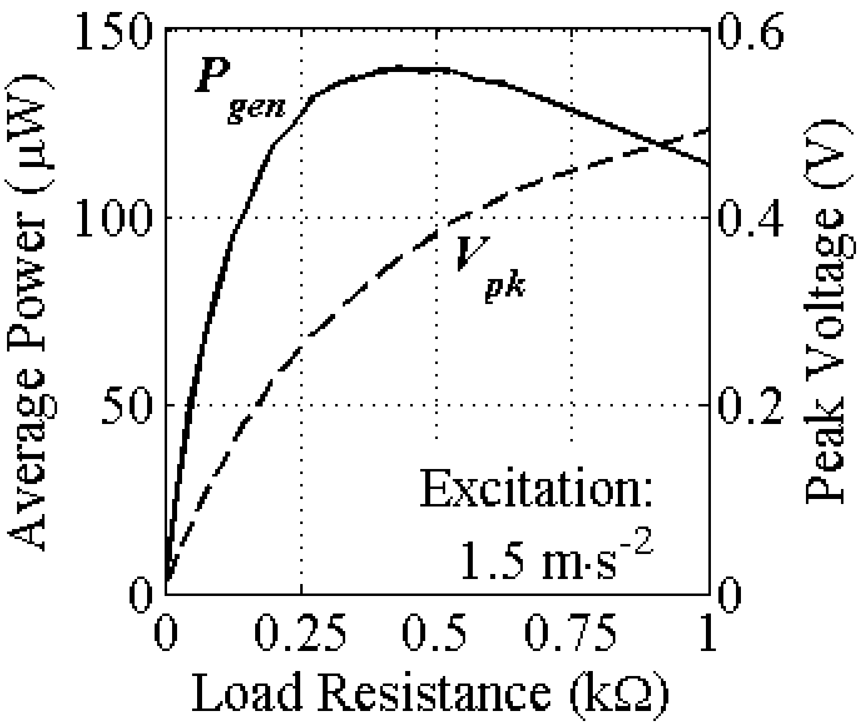


# Slides for Q&A

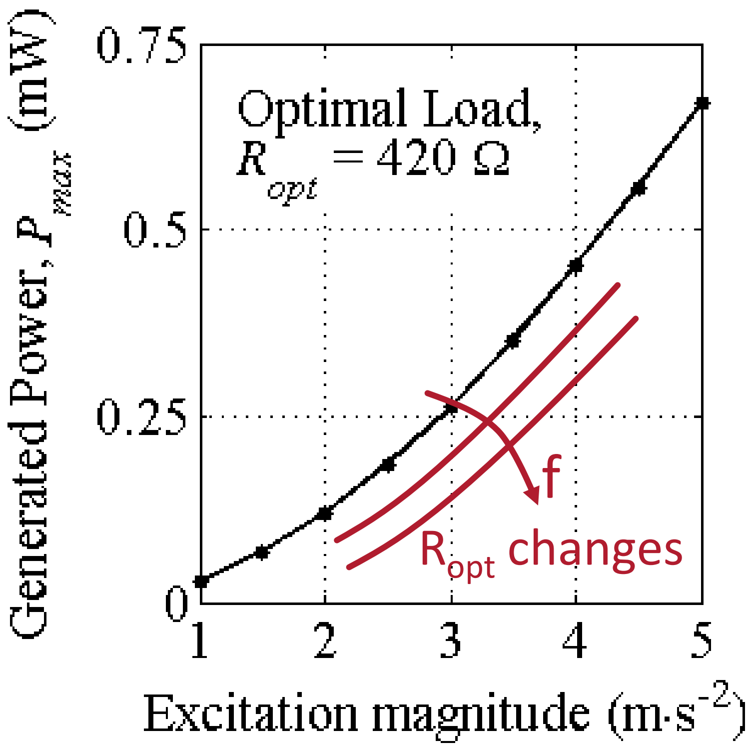

0.5
0.4
0.3
0.2
0.1
0
Stored Energy (J)
0
200
400
600
800
1000
Time (s)
MPTT
Open-loop
δ = 0.67
Passive
Quadrupler
Start up


Output Current, $I_{use}$ (μA)
Duty Ratio, $\delta$
Time (s)
0
100
200
300
400
0.65
0.7
0.75
0.8
0.85
0
2.5
5
7.5
10
12.5
15
$V_{out}$ = 4.5V
$I_{use}$
$\delta$
$V_{out}$ = 2V

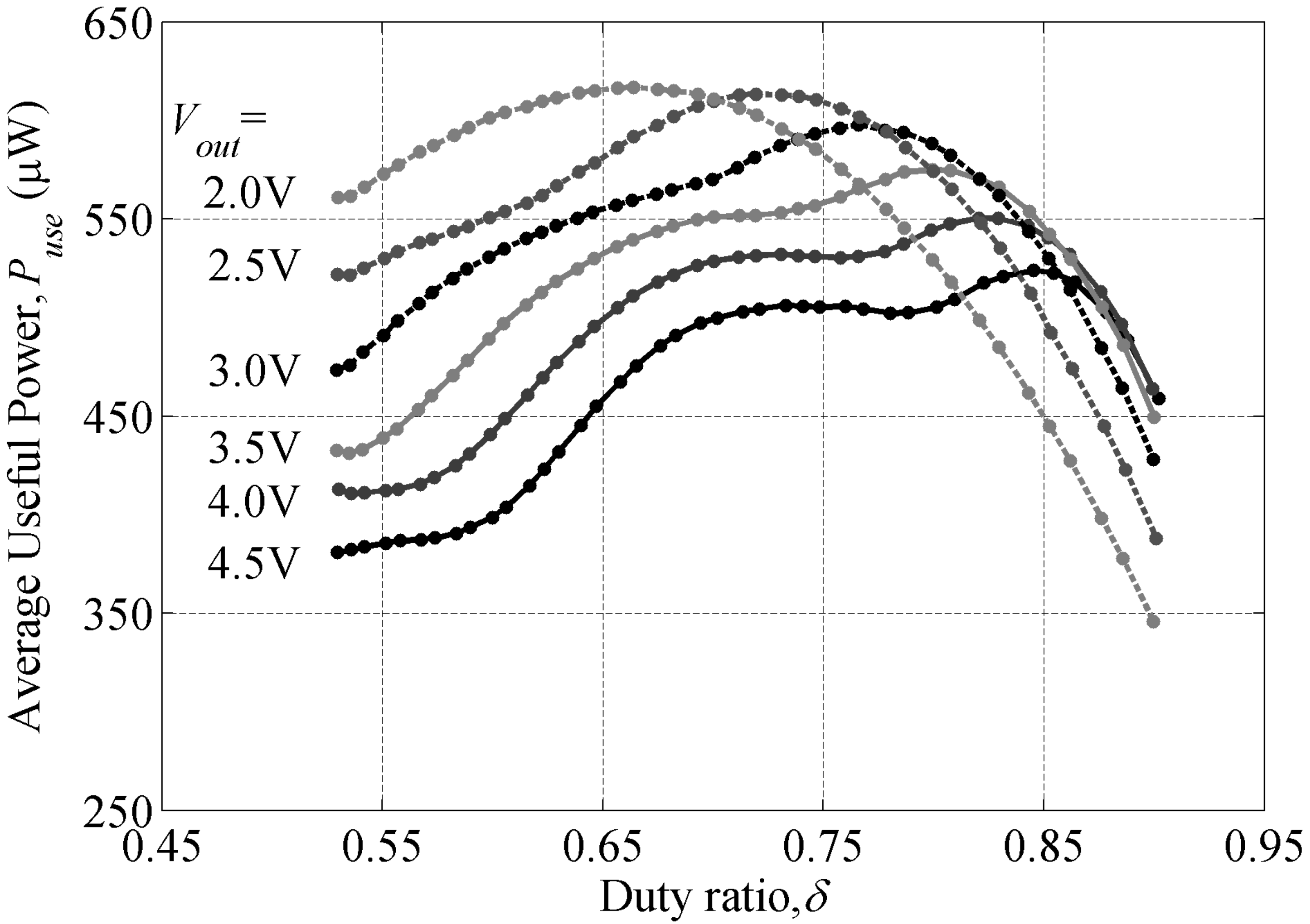

250
200
150
100
0.85
0.8
0.75
0.7
0
2
4
6
8
10
12
Time (s)
Output Current, $I_{use}$ (μA)
Duty Ratio, δ
$I_{use}$
δ


150
100
50
0
0.6
0.4
0.2
0
0
0.25
0.5
0.75
1
Average Power (μW)
Peak Voltage (V)
Load Resistance (kΩ)
$P_{gen}$
$V_{pk}$
Excitation:
$1.5\ m{\cdot}s^{-2}$

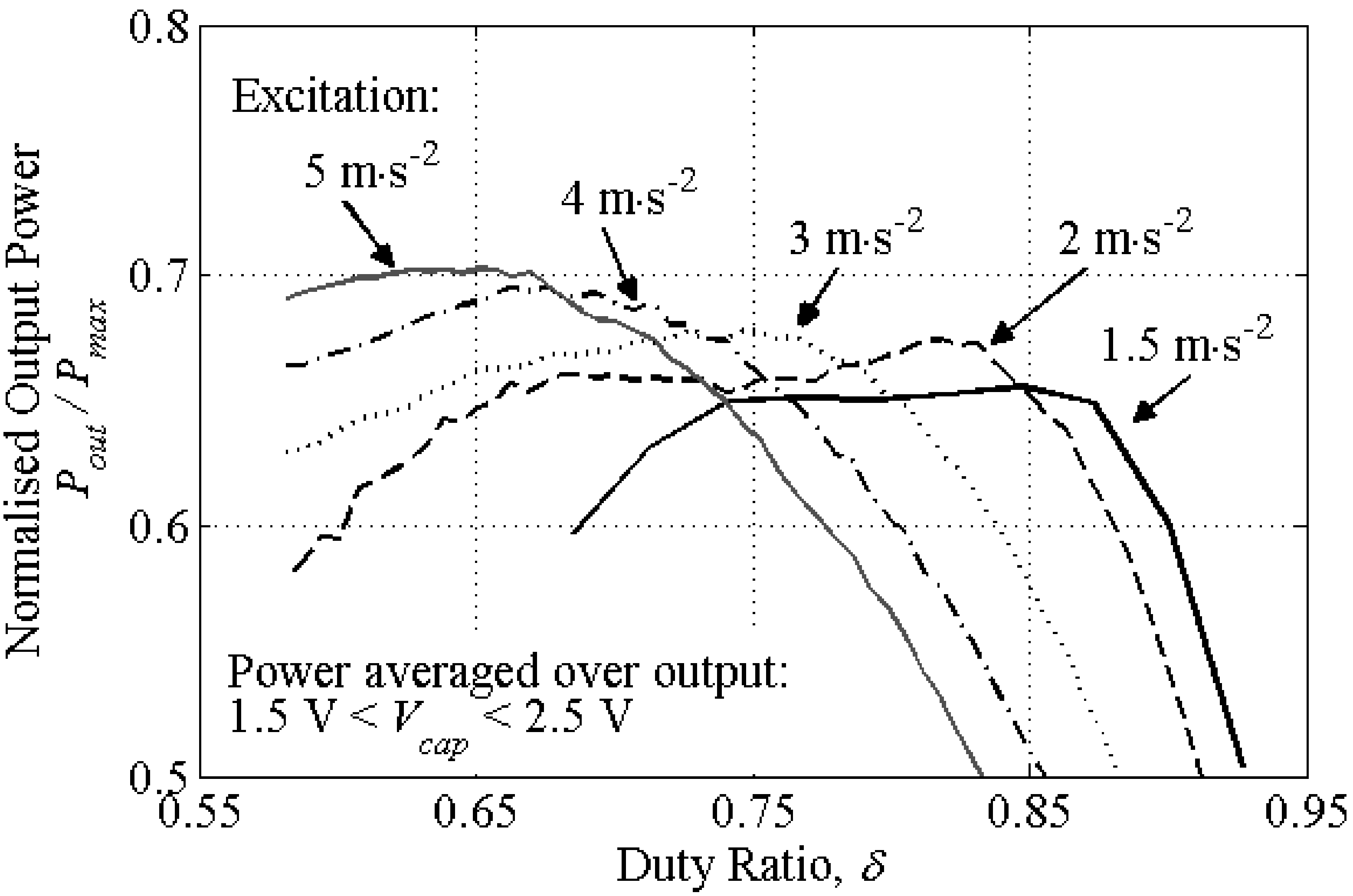
a)


0.75
0.5
0.25
0
1
2
3
4
5
Generated Power, $P_{max}$ (mW)
Excitation magnitude ($m{\cdot}s^{-2}$)
Optimal Load,
$R_{opt}$ = 420 Ω
f
$R_{opt}$ changes

b)



650
550
450
350
250
0.45
0.55
0.65
0.75
0.85
0.95
Average Useful Power, $P_{use}$ (μW)
Duty ratio, $\delta$
$V_{out}$ =
2.0V
2.5V
3.0V
3.5V
4.0V
4.5V


Excitation:
5 m·s$^{-2}$
4 m·s$^{-2}$
3 m·s$^{-2}$
2 m·s$^{-2}$
1.5 m·s$^{-2}$
Power averaged over output:
1.5 V < $V_{cap}$ < 2.5 V
0.8
0.7
0.6
0.5
0.55
0.65
0.75
0.85
0.95
Normalised Output Power
$P_{out} / P_{max}$
Duty Ratio, $\delta$

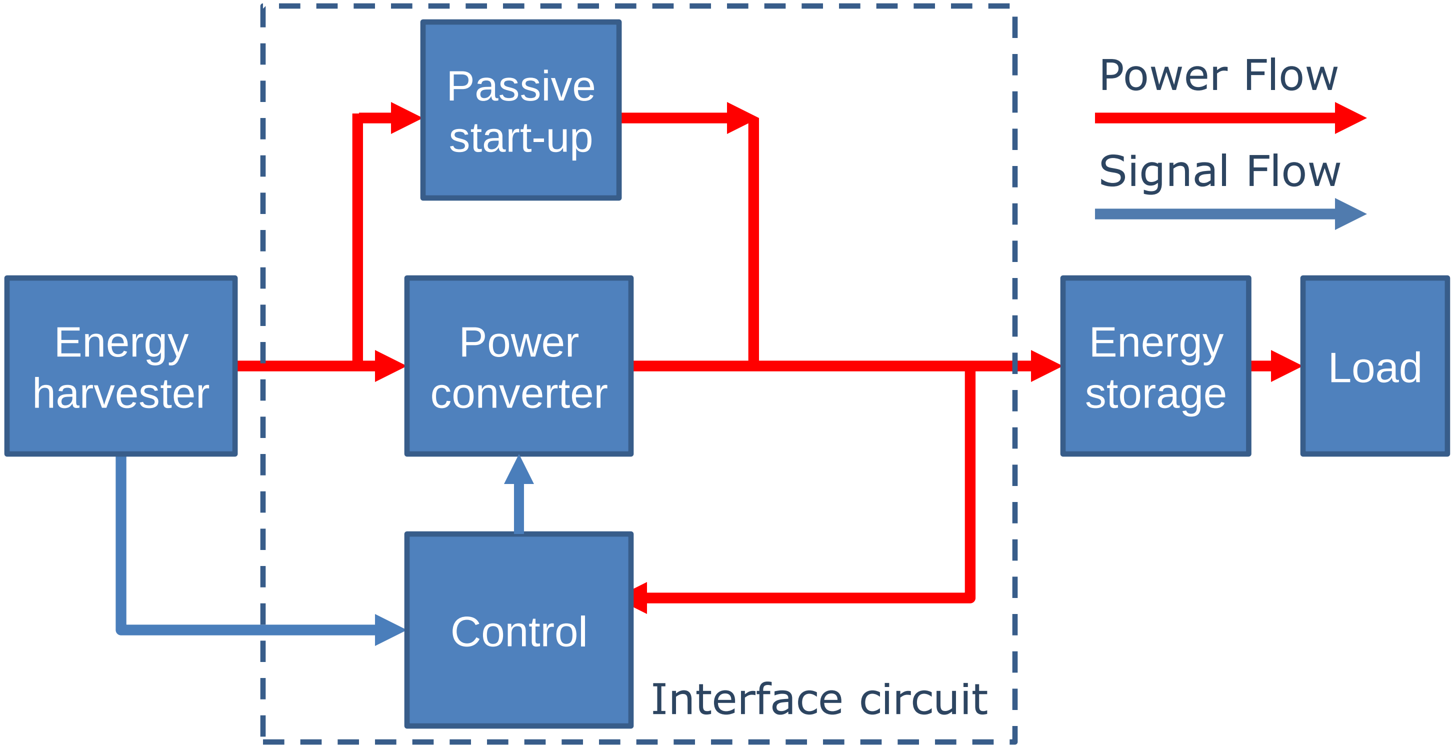
# TASK A2 – INTERFACE CIRCUITRY FOR VIBRATION-DRIVEN ENERGY HARVESTERS

## Main challenges

- Interface circuit design
- Matching circuit behaviour to harvester (impedances)
- Maximum power point tracking
- Tracking amplitude, frequency and load changes
- Very low power implementations

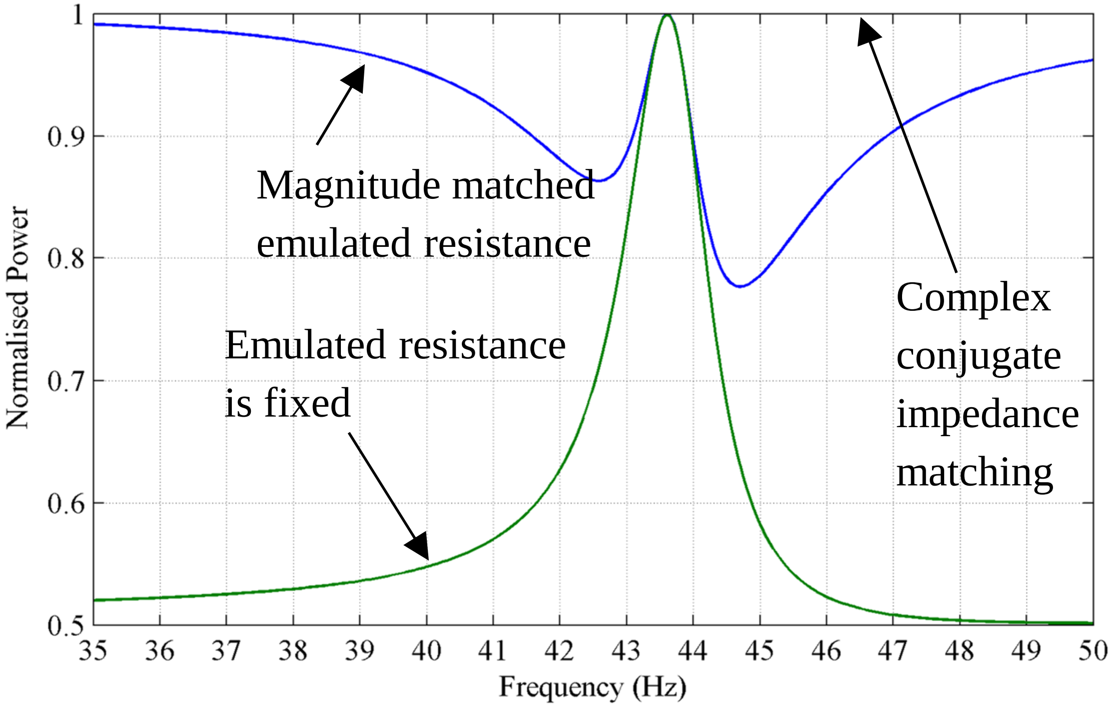
# INTERFACE CIRCUIT DESIGN

- Rectification and Voltage Boosting
  - The harvester generates low-amplitude (<1V) AC voltage
  - The load requires 2V – 4.5V DC voltage
- Zero energy start-up



# MATCHING CIRCUIT INPUT IMPEDANCE TO HARVESTER

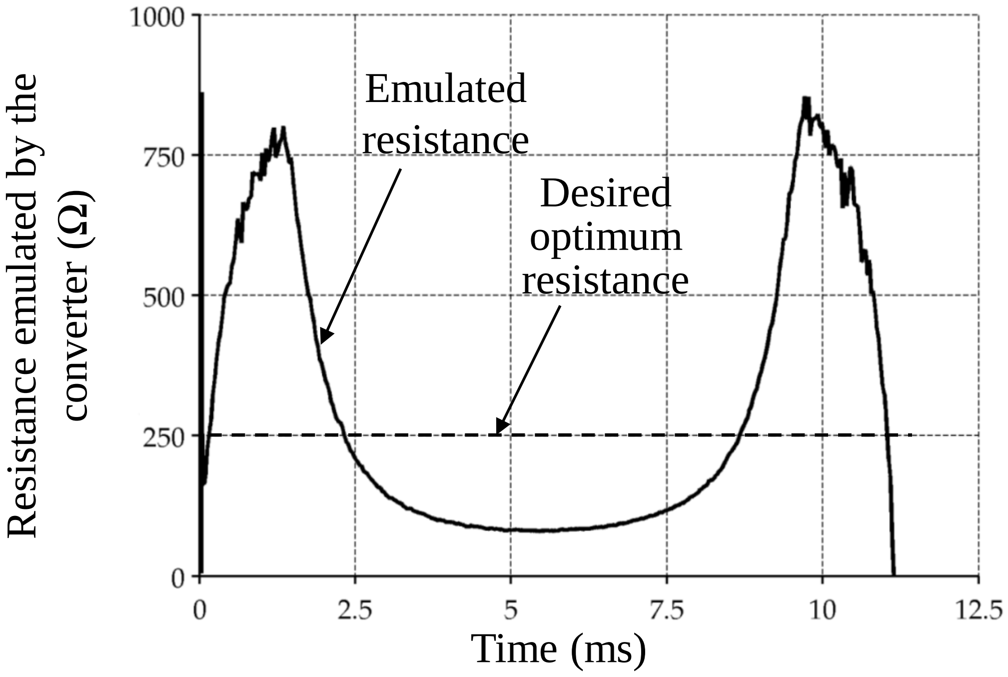
- Maximum power is extracted at matched impedances
- Harvester impedance is a function of the frequency
- Complex conjugate impedance matching requires high quiescent power for implementation
- Power close to the theoretical maximum can be extracted when the emulated resistance matches the magnitude of the source impedance



Power extracted with fixed load (green) and load adaptive to the frequency (blue)

# CONVERTER CONTROL

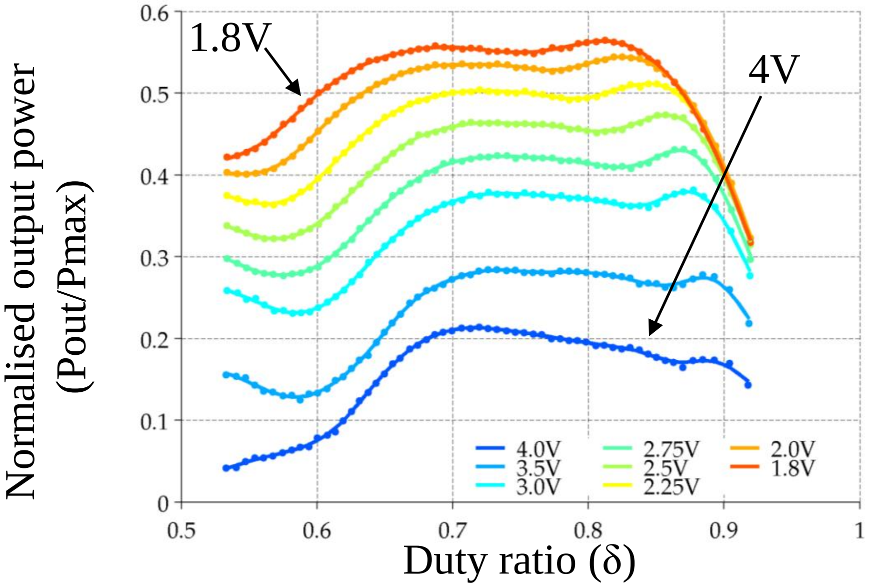
- The input impedance of the converter is a function of the instantaneous input and output voltages
- For maximum power extraction the impedance should be fixed during the harvester cycle and equal to the optimum



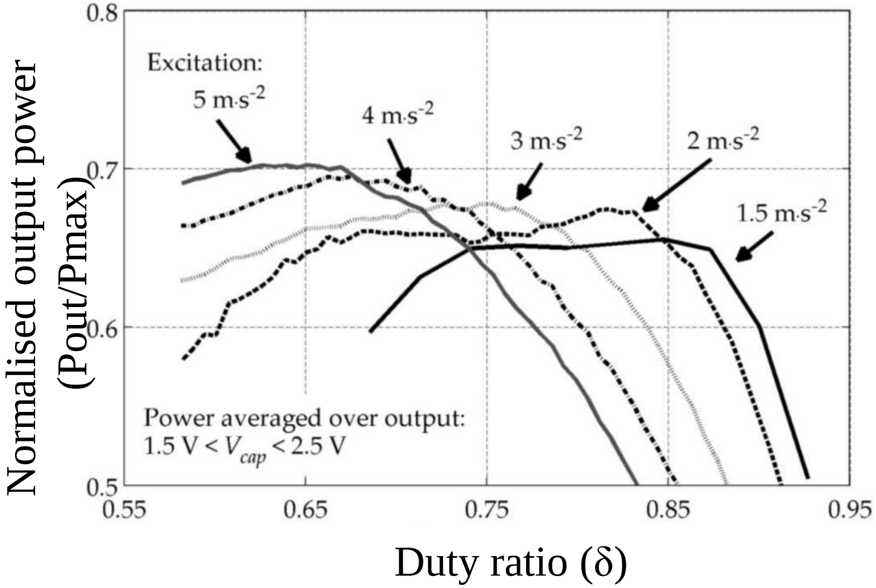
Emulated resistance during one harvester half-cycle at a constant duty ratio of the converter, the variation is caused by variation in the input voltage

# MAXIMUM POWER TRANSFER TRACKING

- The power delivered to the load is a function of the extracted power and the conversion efficiency
- The optimum operating point is a function of the excitation magnitude and the output voltage



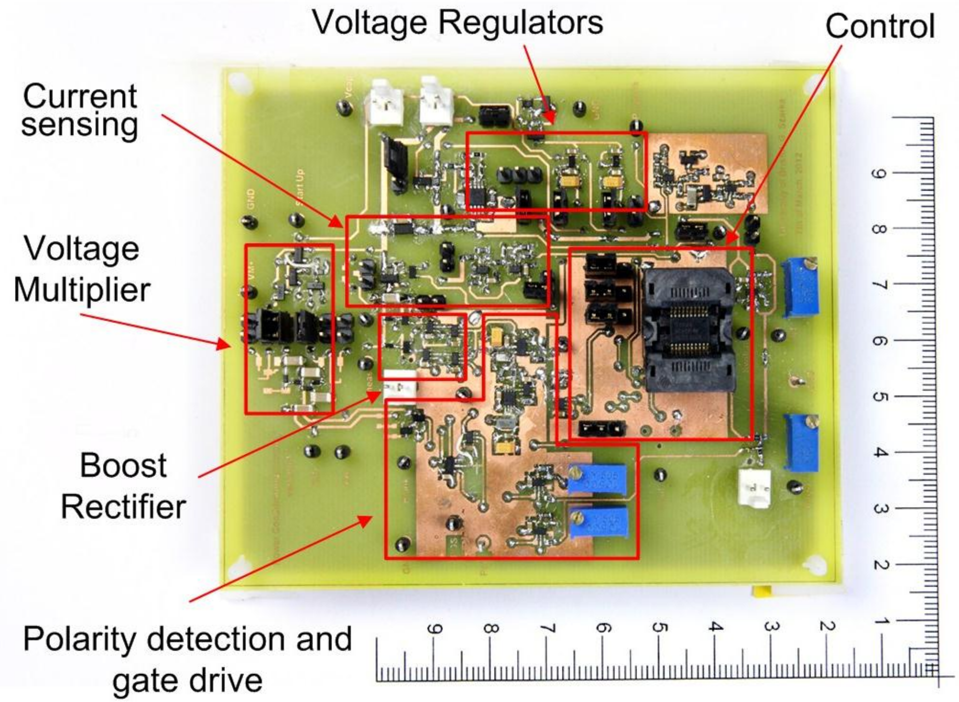
Output power as a function of the duty ratio at different output voltages, acceleration is constant (200 mg)



Output power as a function of the acceleration averaged over output voltage levels from 1.5 to 2.5 V

# LOW POWER IMPLEMENTATION

- All functional requirements should be implemented at very low power which will allow for miniaturization of the harvester
- To achieve low-power operation:
    - The quiescent consumption should be as low as possible
    - The conversion efficiency should be maximised

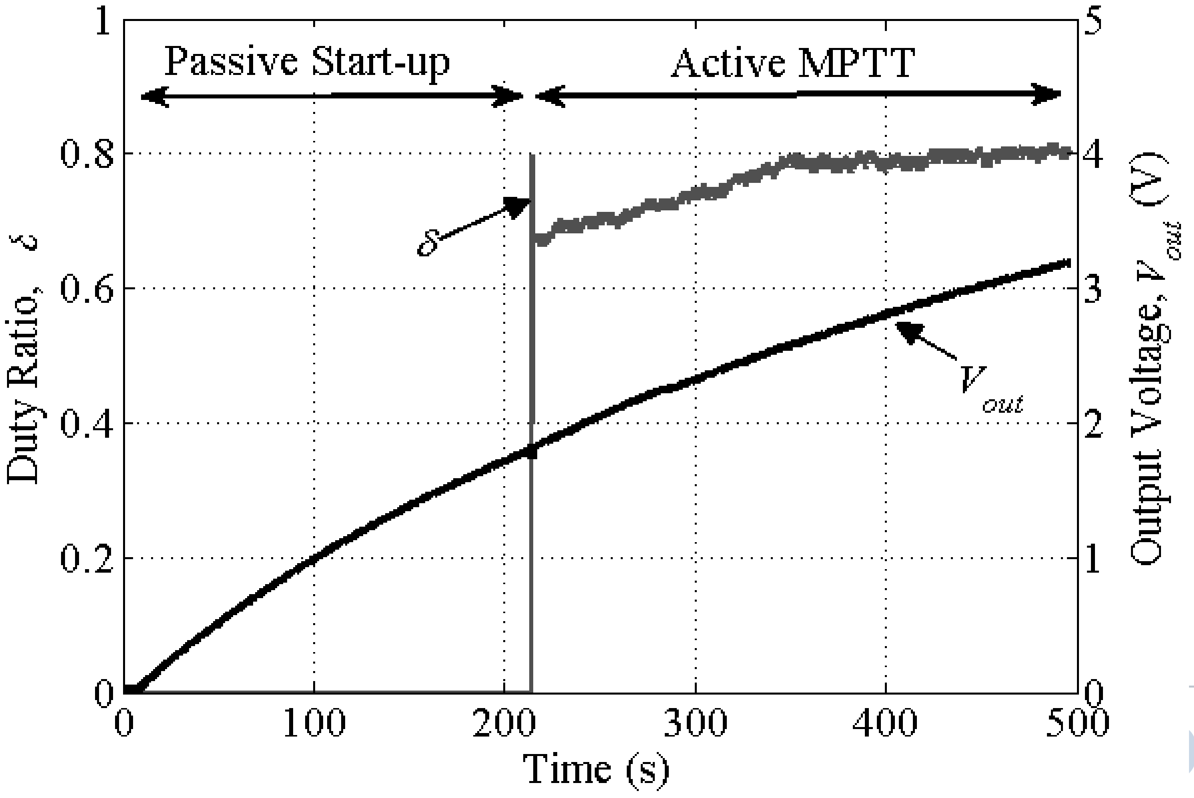


Implementation of high-efficiency ultra-low-power adaptive interface circuitry for energy harvesting

# Power electronics

Adaptive operation example:

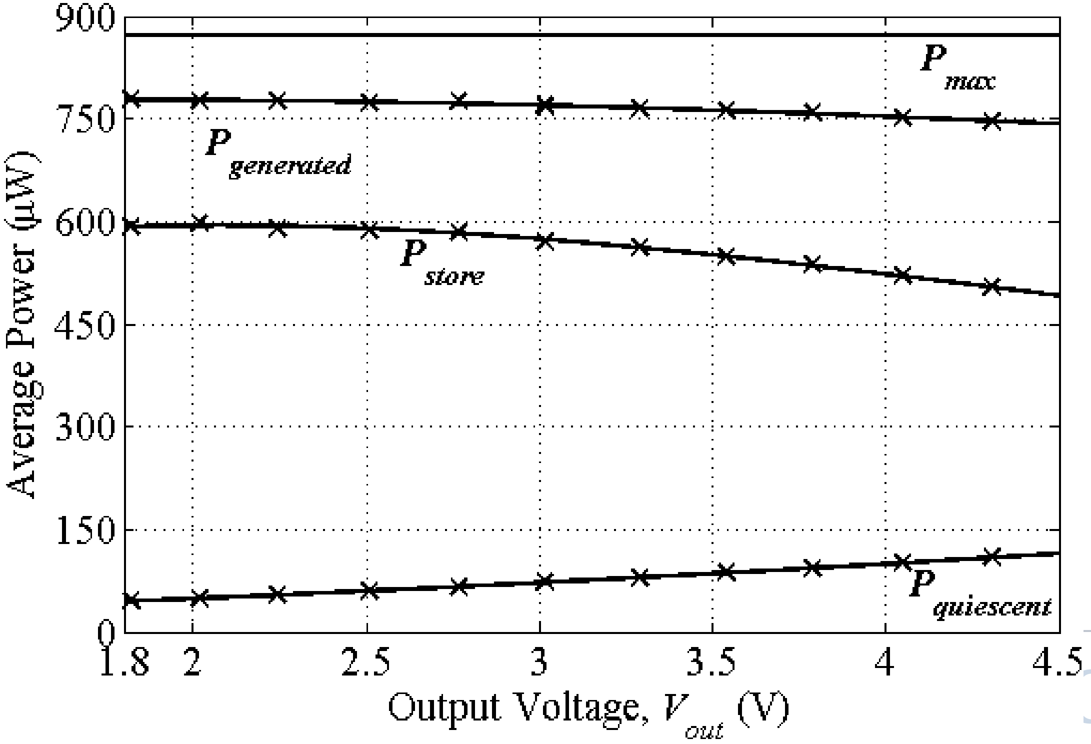
- Acceleration of the input excitation: 3.75 m·s$^{-2}$
- Charging 68 mF capacitor from 0 V to 3.3 V
- The digital control becomes operational at 1.8 V and MPTT finds the optimum duty-ratio



# Power electronics

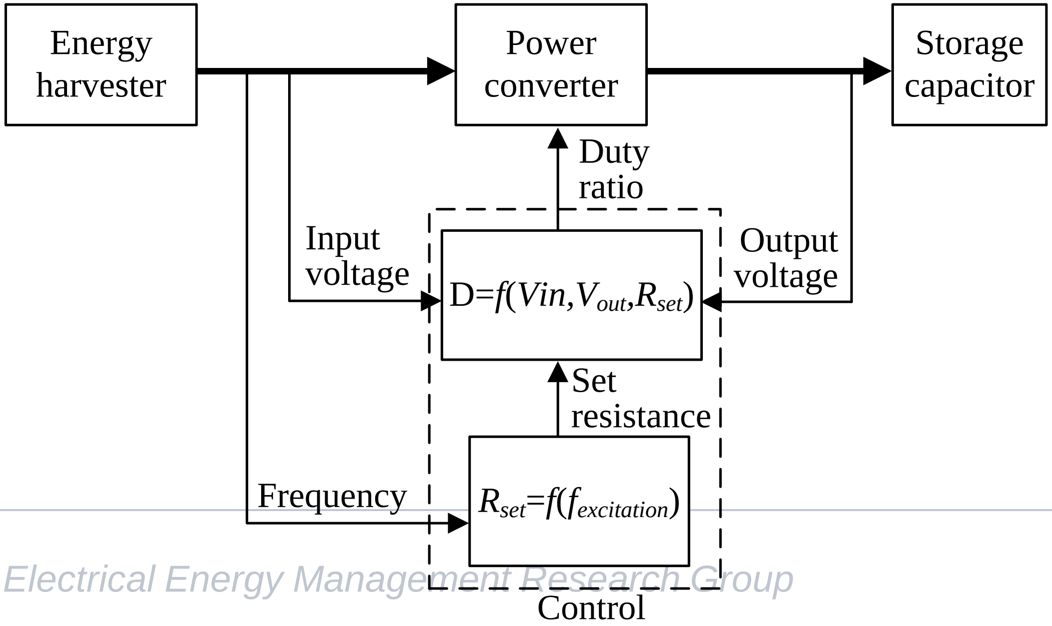
Adaptive operation example:

- Output power is a function of the input power and the efficiency of the converter
- MPTT maximises the output power
- Average overall efficiency (ratio between the output power $P_{store}$ and theoretical maximum power $P_{max}$ ) – 0.7-0.75%



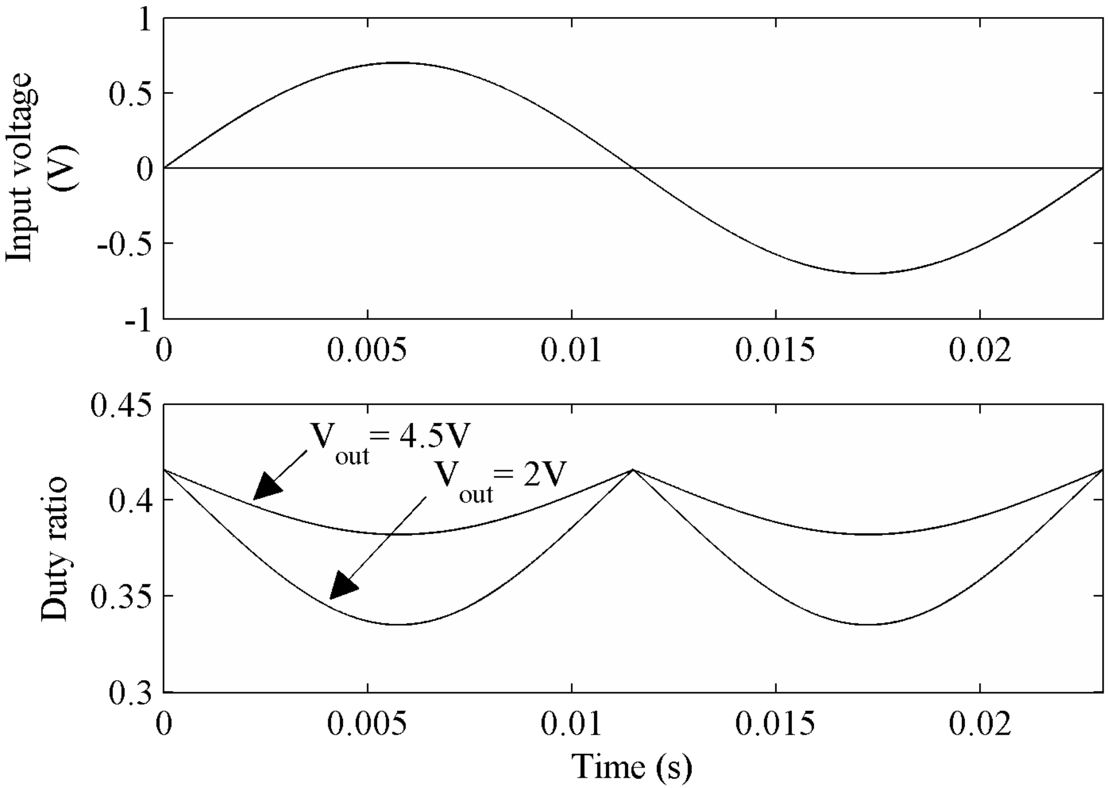
# Improving the adaptiveness of the system

- Instantaneous optimisation corresponding to variations of the input and output voltages – ensures the input resistance of the converter is not affected by variations of the input and output voltages
- Response to changes in the frequency of the excitation – the new optimum point can be determined by measuring the frequency



# Constant resistance emulation

- Duty ratio required to maintain constant resistance during one cycle :



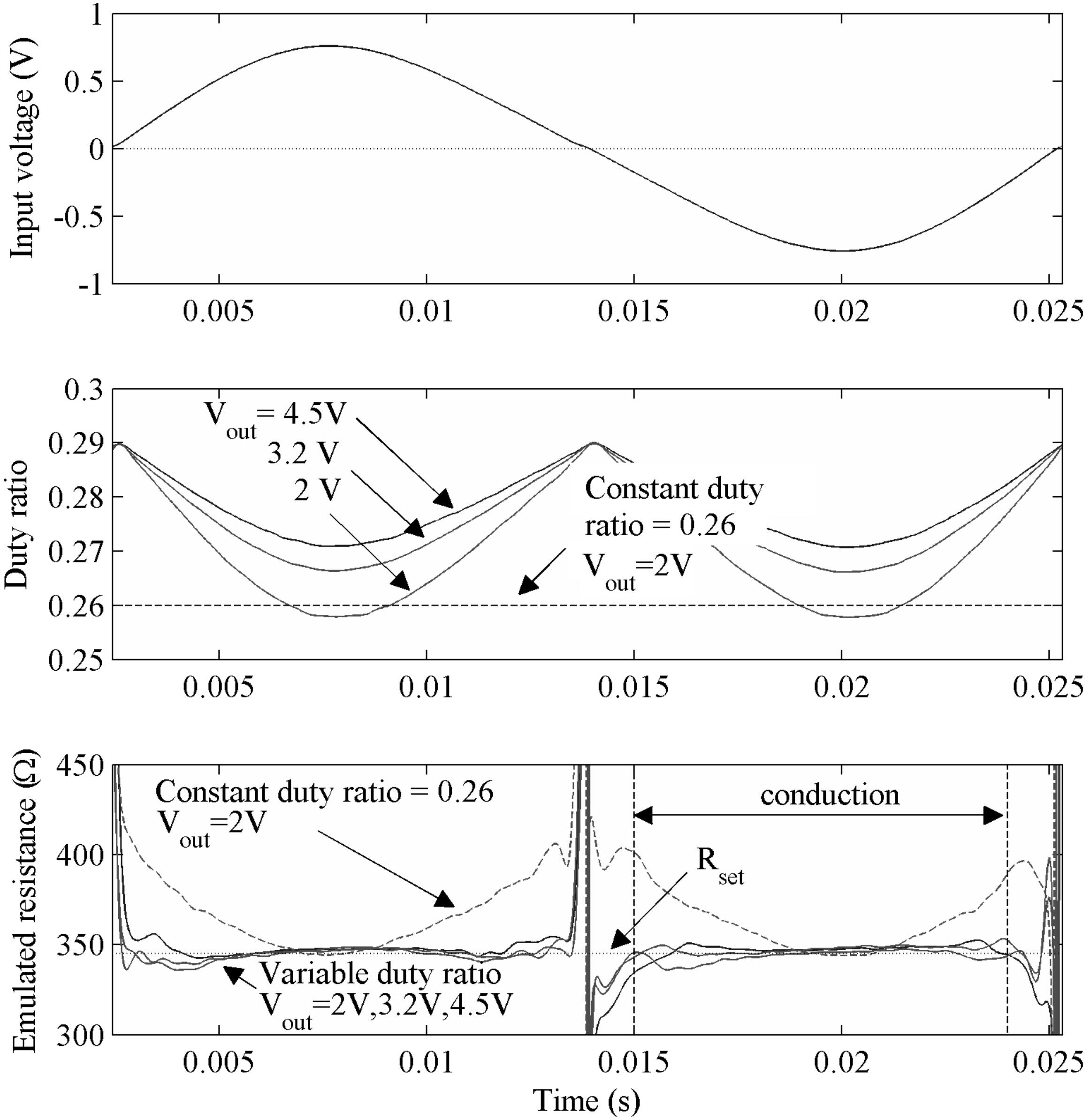
- $V_{in\ pk}$ = 0.6 V
- $V_{out}$ = 2 V,4.5 V

- Maximum variation of the required duty ratio: 17%

# Fixed resistance emulation

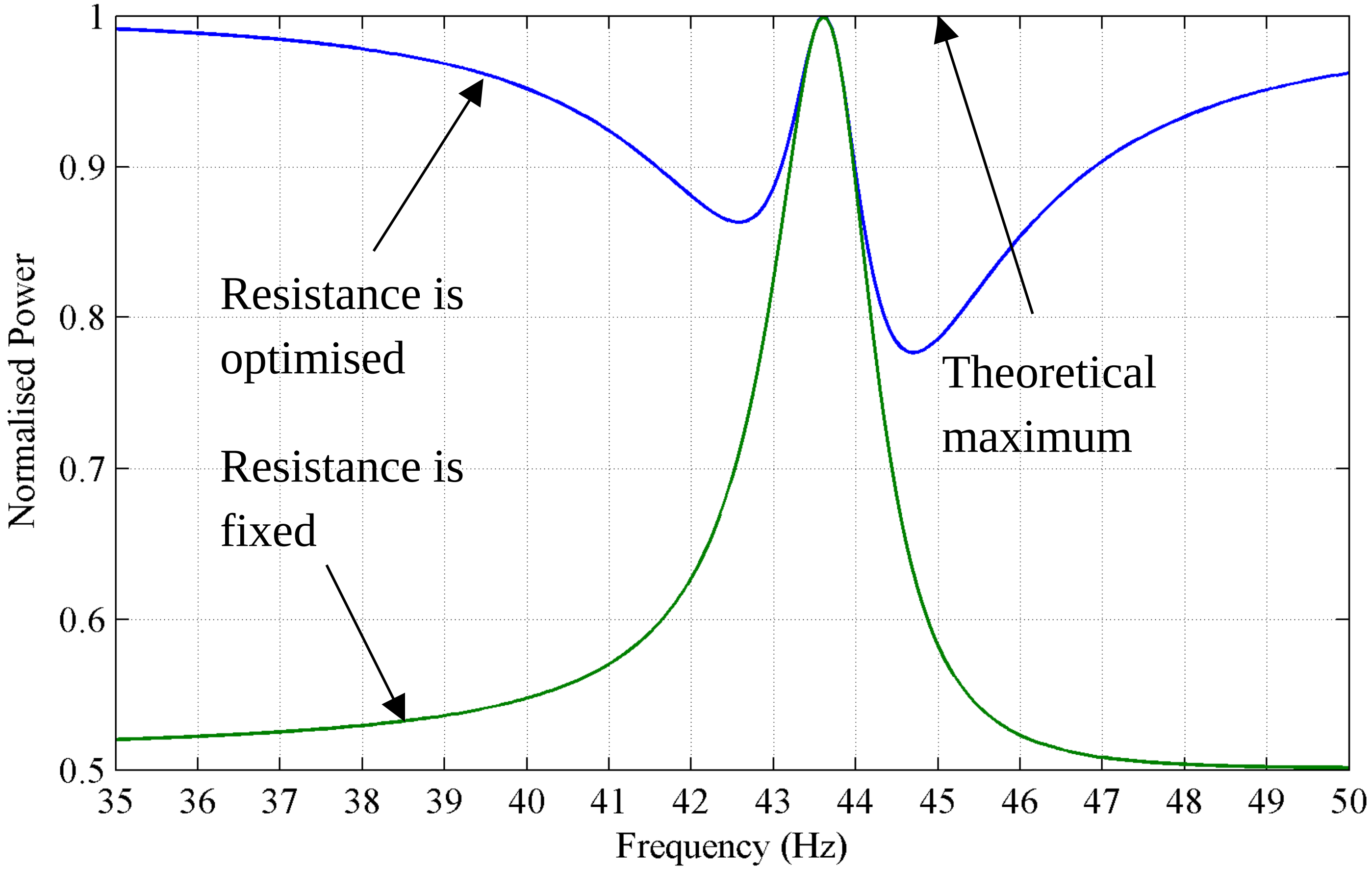
- Emulated resistances for different output voltages with variable duty ratio compared to constant duty ratio

- Constant duty ratio results in 15% maximum deviation from the optimum resistance during the period of conduction



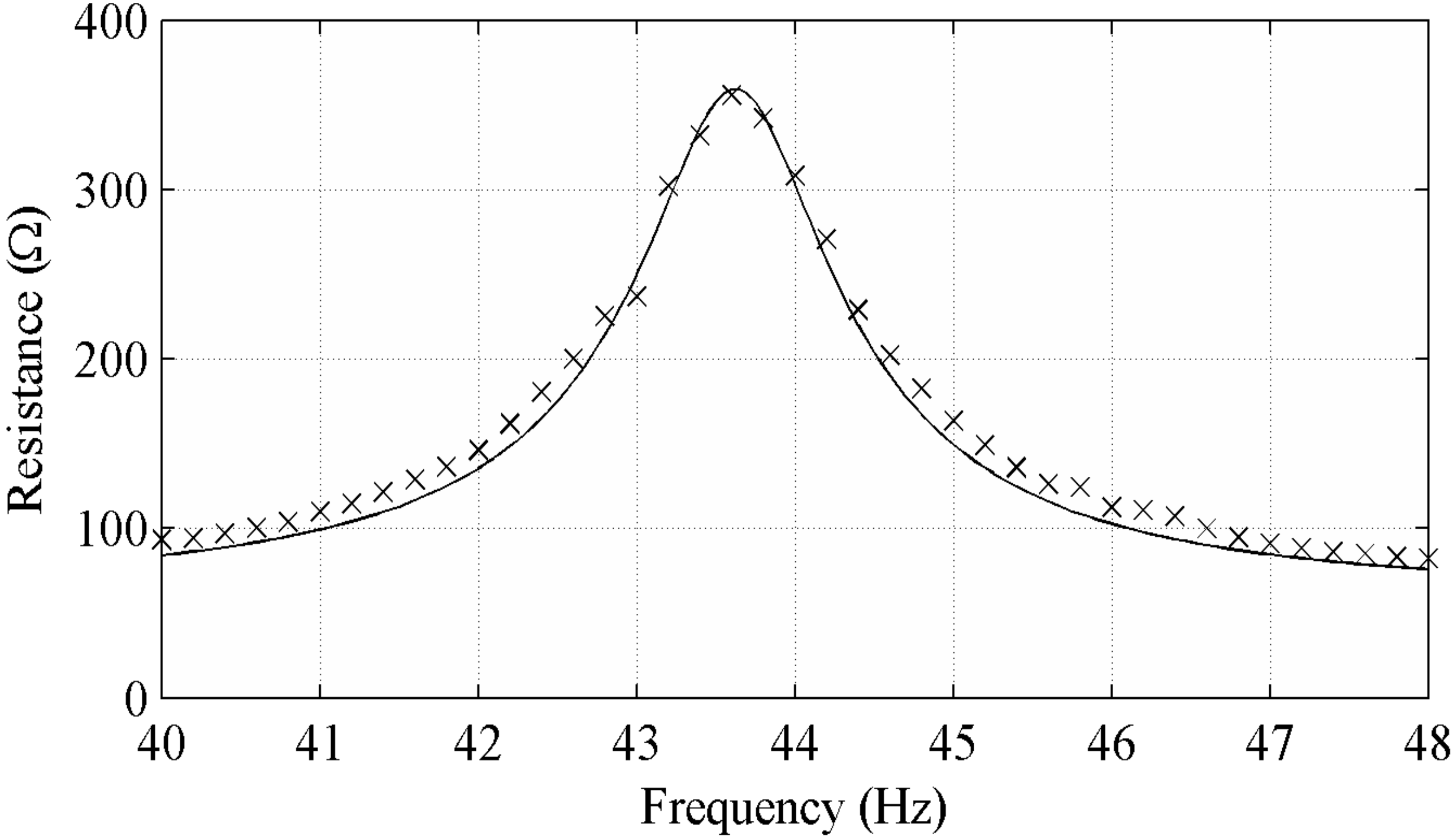
# Magnitude matching

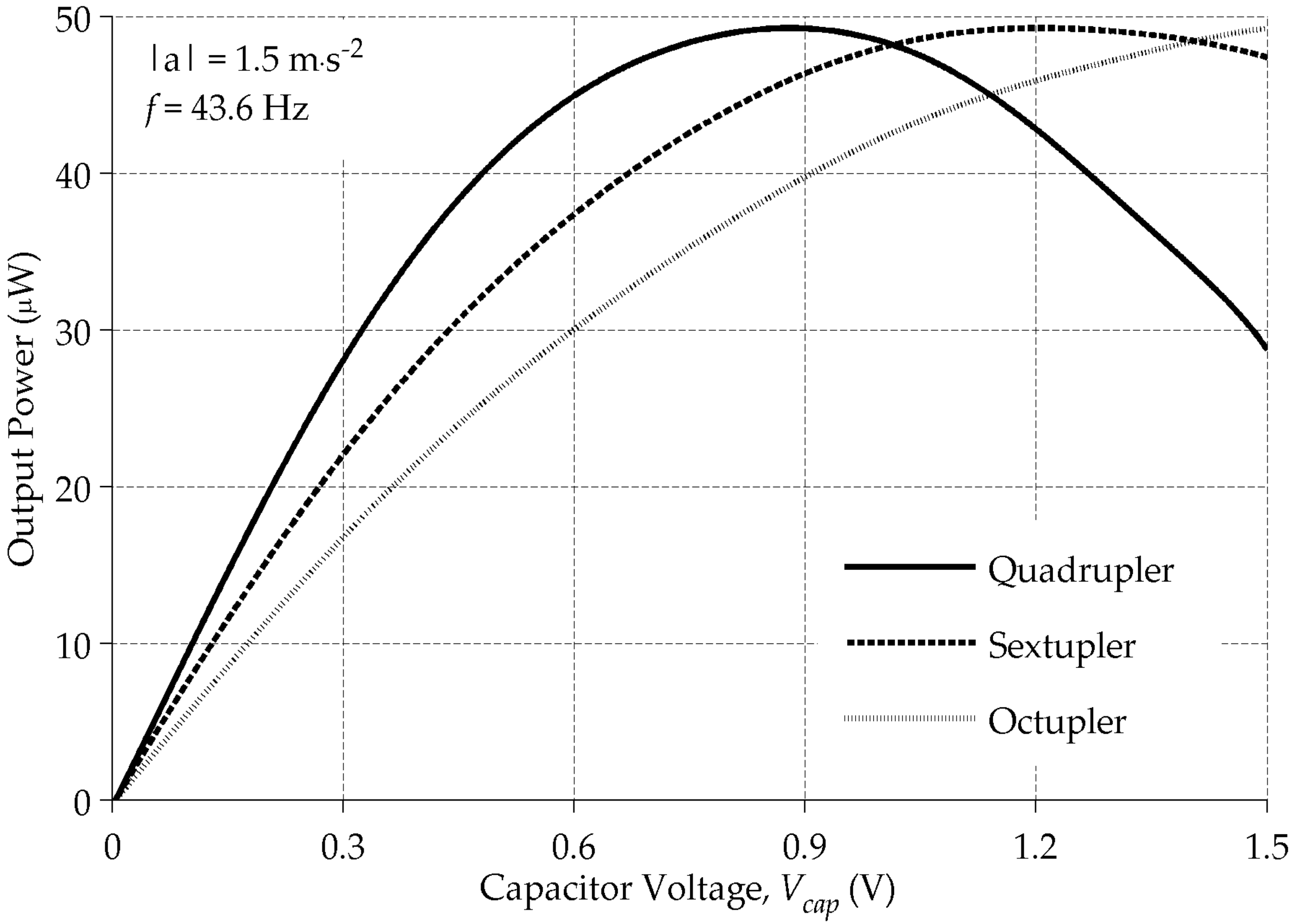
- Optimising the input resistance of the converter to match the magnitude of the source impedance.



# Emulated Resistance

- Measured resistance (×) compared to the theoretical optimal resistance (-) for maximum power extraction with magnitude matching.




|a| = 1.5 m·s$^{-2}$
$f$ = 43.6 Hz
Output Power (μW)
50
40
30
20
10
0
0
0.3
0.6
0.9
1.2
1.5
Capacitor Voltage, $V_{cap}$ (V)
Quadrupler
Sextupler
Octupler