PRiME Power-efficient, Reliable, Many-core Embedded systems

EPSRC Engineering and Physical Sciences Research Council

Hardware-Validated Performance, Power and Energy Modelling of Heterogeneous CPUs – Theme 2

Introduction

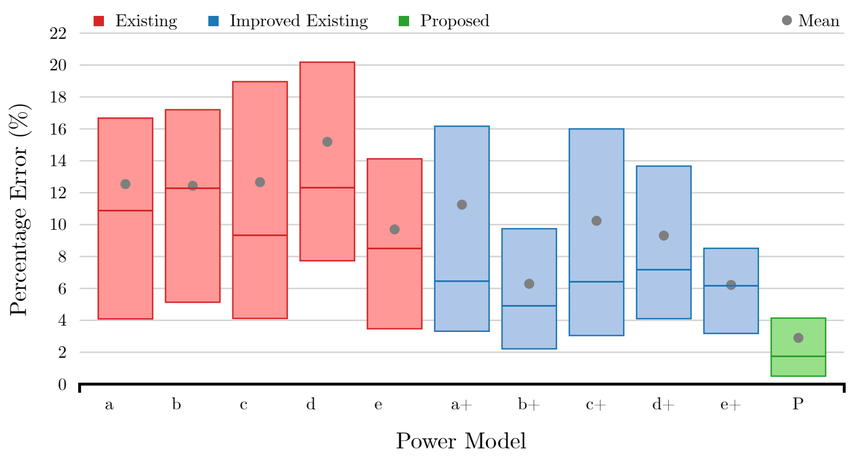
1) Effective run-time system energy-optimisation requires accurate online power estimations
   Problem: existing models do not cope with the wide range of workloads
2) Research and design-space exploration requires representative performance and energy simulators
   Problem: Existing simulators have large errors, which are not understood by users – incorrect research results and conclusions

Accurate and *Stable* Run-Time Power Modelling

Empirical model building methodology focusses on achieving stability in the coefficients, enabling the model to work on a wide range of workloads.

The automated PMC power modelling methodology uniquely:

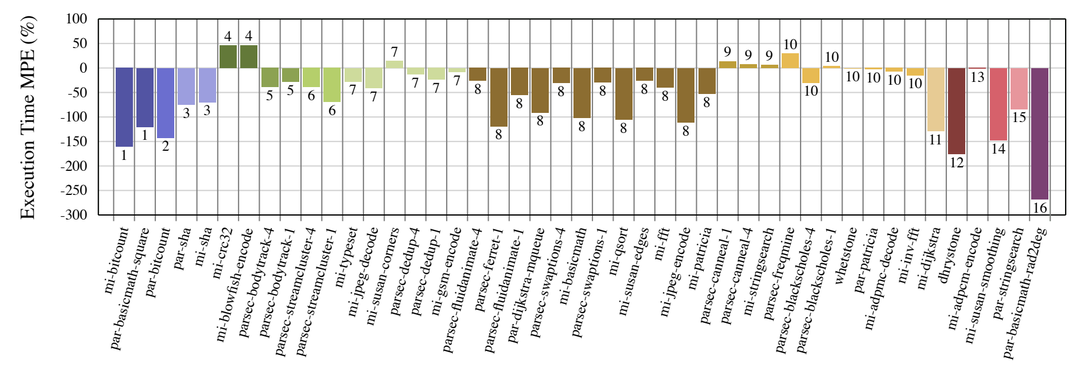
- Reduces multicollinearity using the Variance Inflation Factor (VIF), statistical significance and the coefficient of determination before making input transformations
- Formulated to work at any DVFS level and breaks down static power, dynamic activity power, and the constant dynamic power.
- Raises and overcomes the inherent problem of heteroscedasticity
- Models the effects of the non-ideal behaviour of the voltage regulator and measures the impact on model accuracy
- Models the effects of CPU temperature on the power consumption



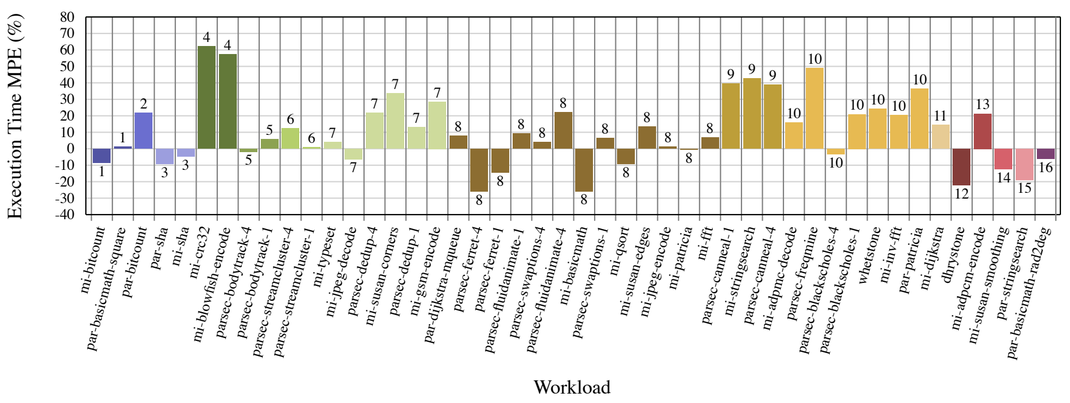
Arm Cortex-A7 MAPE: 3.8%, Arm Cortex-A15 MAPE: 2.7%

Automatic Gem5 Model Hardware-Validation and Error Identification

Compares hardware data with gem5 simulations and uses hierarchical cluster analysis, correlation analysis, regression analysis and microbenchmarks to:
1) Evaluate the accuracy of the model for different types of workloads
2) Identify sources of error for iterative model improvement
3) Allows a user to understand the model's limitations and evaluate its suitability for its intended use-case
4) Enables checking of simulator changes, e.g. the graphs below show two different versions of the same gem5 model (Model A with a bug that went unnoticed).



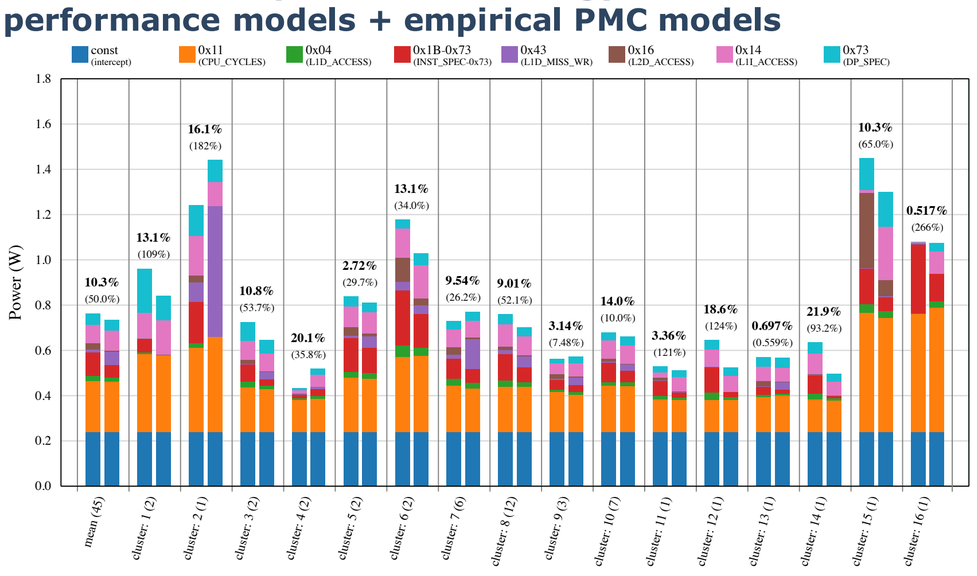
Model A: MPE: -51%



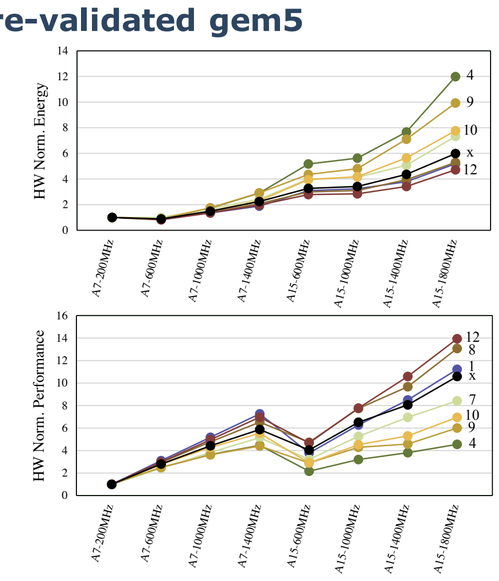
Model B: MPE: +10%

Hardware-Validated Energy Simulation

Accurate and representative energy simulation: hardware-validated gem5 performance models + empirical PMC models



Power model comparison applied to PMC data (left bars) and gem5 Model A data (right) across different workload clusters.



Validation of performance and energy scaling across DVFS level and microarchitectures

Conclusion

Novel methodologies for:
1. building accurate and stable run-time power models, and
2. automatically validating gem5 models against hardware and identifying sources of error.

The result is accurate run-time power estimation for run-time management and representative system simulation for design-space exploration.

Six open-source software tools for:
1. Recording PMC data for both ARMv7 and ARMv8 architectures
2. Automating the running of experiments on hardware (workloads, core masks, DVFS recording data, etc.)
3. Building power models using the full presented methodology
4. Automating the running of gem5 experiments
5. Combining gem5 and hardware data, applying analysis and identifying sources of error
6. Applying power models to experiment data and/or gem5 data for energy analysis

powmon.ecs.soton.ac.uk

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